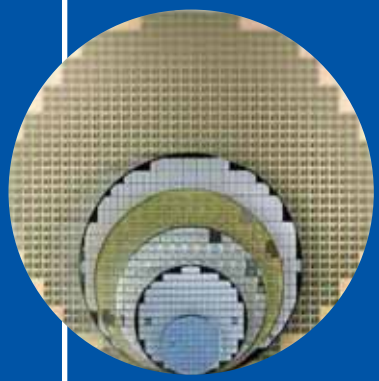

2005 Strategic Research Agenda

European Nanoelectronics Initiative Advisory Council

niac

Strategic Research Agenda

European Technology Platform Nanoelectronics

First Edition, November 2005

ENIAC Executive Steering Committee

Pasquale Pistorio	STMicroelectronics
Wolfgang Ziebart	Infineon
Frans van Houten	Philips
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Arthur van der Poel	MEDEA+
Gilbert Declerck	IMEC
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Ben Ruck	Netherlands
Peter Zangl	European Commission
Ezio Andreta	European Commission

Content

Foreword

This document was prepared by the ENIAC Working Group for the Strategic Research Agenda on behalf of the ENIAC Steering Committee. It is the extended and detailed successor of the Executive Summary presented at the European Nanoelectronics Stakeholder Forum on April 27, 2005, in Brussels. The Strategic Research Agenda will be revised every two years, with interim updates to be issued when needed.

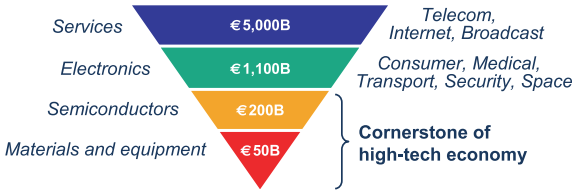
The Strategic Research Agenda is the concerted action of experts from industry, academia, and public authorities across the European Union. Special acknowledgements go to the ENIAC Domain Team leaders Michel Brillouët (CEA/Leti), Norbert Lehner (Infineon), G.Q. Zhang (Philips), Herbert Reichl (Fraunhofer Gesellschaft), Rob Hartman (ASML), Philippe Magarschack (STMicroelectronics), and to the many other contributors, including Alexander Sedlmeier, André Montree, Andrea di Matteo, Bernard Candaele, Bram Jongepier, Carlo Cognetti, Carlos Mazure, Chris van Hoof, Dieter Gräf, Dirk Gravesteijn, Dominique Pons, Dominique Thomas, Eric Beyne, François Xavier Doitteau, Franki d'Hoore, Fred Roozeboom, Gérard Matheron, Gian Guido Rizzotto, Giles Casanova, Hans Boeve, Harald Pötter, Heiner Ryssel, Herbert Roedig, Ingo Höllein, Ivo Raaijmakers, Jan Hendrik Peters, Jean Friedt, Jean-Luc Morand, Jean-Pierre Joly, Jim Greer, Johan Vounckx, Joseph Borel, Jürgen Wolf, Karen Maex, Klaus Bernhardt, Klaus Kronlof, Klaus Pressel, Lambert van den Hoven, Laurent Gouzènes, Livio Baldi, Lode Lauwers, Lothar Schrader, Marcus Schumacher, Mareike Klee, Marie-Noëlle Semeria, Markus Schwerd, Markus Wabro, Mart Graef, Michael Mikulla, Olaf Fortange, Peter van Staa, Pierre Puget, Pietro Erratico, Ralf Plieninger, Reinhard Neul, Roberto Bez, Roger De Keersmaecker, Rolf Aschenbrenner, Rudy Lauwereins, Thijs Viegers, Wolfgang Müller, and Xavier Baraton.

Fred van Roosmalen
Chairman of the ENIAC Working Group for the Strategic Research Agenda

Barcelona, November 23, 2005

Introduction

The semiconductors industry and its suppliers are the cornerstone of today's high-tech economy. Representing a worldwide sales value of 250 billion euro in 2004, the sector supported a global market of more than 6 trillion euro in terms of electronic systems and services, with applications ranging from transportation to health care, and from general broadcasting to electronic banking.



Semiconductors underpin 6 trillion euros worth of electronics and services

Semiconductors have pervaded our lives in the past fifty years. Without it, the rich multimedia experience that we enjoy in today's world of CD, MP3, DVD, and the internet would not have been possible. Without it, we would not be able to talk to people around the world, exchange messages or share photographs and video clips via a personal portable device that fits into our top pocket. Without it, our cars would do far fewer kilometres per litre of fuel, heavily pollute the environment and cause more accidents.

The shift from the past era of microelectronics, where semiconductor devices were measured in microns (1 millionth of a meter) to the new era of nanoelectronics where they shrink to dimensions measured in nanometers (1 billionth of a meter) will make the semiconductor sector even more pervasive than it is today. It will allow much more intelligence and far greater interactivity to be built into many more everyday items around us, with the result that silicon chip technology will play a part in virtually every aspect of our lives, from personal health and traffic control to public security.

As semiconductor solutions become ever more pervasive, the associated value in products will increase both in terms of hardware and software. The epitome of that today is the mobile phone – almost 100% silicon-based content plus one printed circuit board, a battery and a plastic case. Mobile telephony is already a success story for Europe. The most widely adopted mobile communications standard in the world, GSM, was developed and rolled-out from here.

If the era of microelectronics has achieved all this, the new era of nanoelectronics promises much more. It will not only expand the pervasiveness of silicon solutions, making them small enough, light enough and cheap enough to build into just about anything – even disposable products. It will give next-generation products totally new capabilities that will elevate the ICT (Information and Communication Technology) society to unprecedented levels, and it will enable Europe to realize its vision of Ambient Intelligence – living environments that are aware of our presence and responsive to our needs.

The ENIAC vision

A far-sighted strategy for the European nanoelectronics industry, aimed at securing global leadership, creating competitive products, sustaining high levels of innovation and maintaining world-class skills within the European Union is outlined in 'Vision2020 – Nanoelectronics at the Centre of Change' published by the European Commission. In addition to identifying the technological, economic and societal advantages of establishing Europe as a global leader in nanoelectronics, the 'Vision2020' document clearly highlights the importance of creating effective partnerships in order to achieve this goal.

Europe must not only have access to leading-edge technologies for nanoelectronics. It must also have an efficient means of knowledge transfer between R&D and manufacturing centres in order to turn this technology into leading-edge value-added products and services. Such partnerships will therefore need to include all stakeholders in the value chain, from service providers at one end to research scientists at the other, so that nanoelectronics research can remain strongly application focused.

To create an environment in which these partnerships can flourish, 'Vision2020' proposes the development of a European Technology Platform (ETP) and a Strategic Research Agenda (SRA) for nanoelectronics that will enable industry, research establishments, universities, financial organisations, regional and Member State authorities and the EU to interact to provide the resources required, within a visionary program that fosters collaboration and makes best use of European talent and infrastructures. ENIAC (the European Nanoelectronics Initiative Advisory Council) has been set up to define and develop this Technology Platform and Strategic Research Agenda.

The ETP Nanoelectronics encompasses a comprehensive suite of hardware and silicon-centric technologies that firmly underpin the semiconductor sector. The organisation and technology platform corresponding to ENIAC and the ETP Nanoelectronics at the software level are ARTEMIS and the ETP Embedded Systems, which covers the software- and architecture-centric group of technologies in the ICT arena. Together, these two ETPs are the key enablers for future development of the European high-tech economy, providing underlying technologies for virtually all of Europe's other major technology platforms.

Taking into account the short-, medium- and long-term challenges faced by Europe in realizing its vision of the ICT Society and Ambient Intelligence, the ENIAC Strategic Research Agenda identifies and quantifies the performance parameters needed to measure the progress of nanoelectronics research, development and industrialization. By setting these out as a series of clear, application-driven technology roadmaps it will provide guidance in the coordination of local, national and EU wide resources – in the form of research, development, manufacturing, and educational governance, infrastructures and programs – to achieve European success in nanoelectronics. By matching technology push from the scientific community with the innovation of SMEs (Small and Medium-sized Enterprises) and the market pull of large industrial partners and end-users, the Strategic Research Agenda ensures that research coordinated under it is industrially, economically and societally relevant. A formal on-going review process will make the agenda adaptive to events such as changing market and societal conditions or the emergence of disruptive technologies.

Benefits for Europe

Europe possesses an effective infrastructure for the development and production of semiconductor technologies. Two of Europe's wafer fabs (Crolles in France and Dresden in Germany) are currently producing 90-nm CMOS devices on 300-mm diameter wafers, which is state-of-the-art in the industry. Europe also has some of the world's foremost centers for semiconductor research in the form of IMEC (Belgium), CEA-LETI (France) and Fraunhofer VME (Germany).

From a technological point of view this puts Europe in a strong position to realize its visions in the areas of Information and Communication Technology and Ambient Intelligence. Key to this success will be maintaining Europe's world leadership as semiconductor manufacturing moves deeper and deeper into the nanoelectronics world. Maintaining this leadership will ensure that critical intellectual property in the area of nanoelectronics is generated and benefited from in Europe. It will not only create a pool of industrially focused research engineers. It will create highly skilled jobs in the resultant semiconductor, systems integration, product design, product manufacturing and service sectors. In particular, it will further reinforce Europe's existing strength in areas such as telecommunications, medical and automotive electronics.

Nanoelectronics is a key enabler in building a sustainable economy for Europe. It is a major driver for innovation in the research and implementation of essential components and design skills for embedding in high-technology systems worldwide. It will ensure the continued employment of highly-skilled workers in knowledge-based industries, creating as many as ten indirect jobs for every direct worker in the nanolectronics industry itself. It will promote infrastructures in which industry will stimulate innovation-focused scientific research and training, and where large industrial players will foster SMEs and start-ups in emerging segments of the overall economic value chain. A thriving nanoelectronics industry is therefore an essential component in determining the shape and direction of Europe's future.

Society needs drive applications

The society of the future expects environments that are sensitive and responsive to the presence and needs of people, characterized by many invisible devices distributed throughout the environment. Devices that know about their situational state, that can recognize individual users, tailor themselves to each user's needs, and anticipate each user's desires without conscious mediation. In other words, environments based on the concept of Ambient Intelligence.

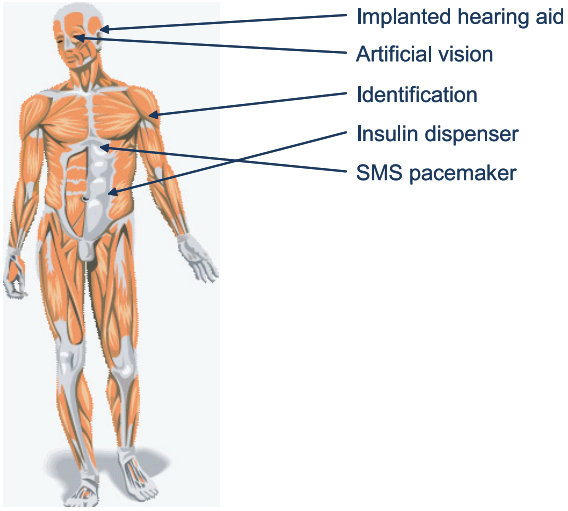
In the world of Ambient Intelligence, ENIAC has recognized five application domains, each of them driven by clearly recognizable societal needs:

- Health
- Mobility / Transport
- Security / Safety
- Communication
- Education / Entertainment

The Strategic Research Agenda translates each of these domains into technical requirements, thereby outlining the key challenges and roadblocks to be resolved in order to reach integrated intelligent Nanoelectronic solutions.

Health

With the advent of nanotechnology, medicine will undergo a revolution. Fast, highly sensitive DNA/protein assays made possible by innovative new bio-sensors will allow many diseases to be diagnosed 'in-vitro' from simple fluid samples (blood, saliva, urine etc.) even before sufferers complain of symptoms. Similar tests will identify those pre-disposed to certain diseases, allowing them to enter screening programs that will identify early onset of the disease. Conventional and molecular imaging, increasingly combined with therapy, will pinpoint and eradicate diseased tissue. Early diagnosis will lead to earlier treatment, and earlier treatment to better prognoses and after-care. By 'nipping disease in the bud' it will make many therapies either non-invasive or minimally invasive. And equipped with body-sensors that continuously monitor their state of health and report significant changes through tele-monitoring networks, patients will be able to return home sooner and enjoy a faster recovery. Nanomedicine will also revolutionise prosthetics, with bio-implants restoring sight to the blind and hearing to the deaf. Automated drug-delivery implants will prevent conditions such as epileptic fits.



Intelligence applied: silicon meets carbon

For developers of the nanoelectronic systems that will lie at the heart of many of these developments, it will pose many challenges, such as the bio-compatibility of the materials they use both for in-vitro and in-vivo applications, and the maximum thermal load that implanted devices can impose on the human body. In some cases, biosensors will have to achieve phenomenal sensitivities, equivalent to detecting the presence of a grain of salt in an Olympic swimming pool. Developing implants in bio-compatible packages will push System-in-Package (SiP) miniaturisation

to the limits, while at the same time having to cope with the integration of devices such as biological sensors, Nano Electro-Mechanical System (NEMS)/mechatronics devices, optical devices, energy scavenging systems and RF interfaces. At the same time many of these highly complex heterogeneous systems will have to provide life-support system reliability.

Mobility / Transport

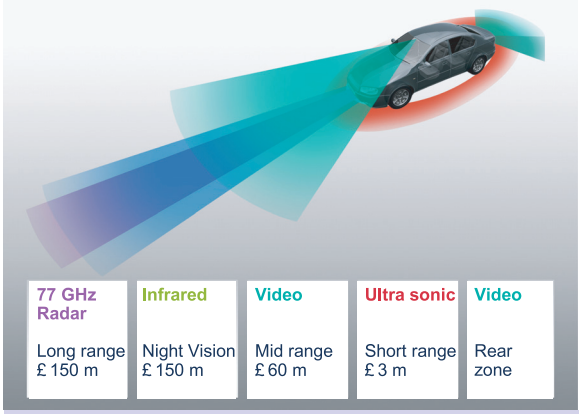
As the volume of traffic on our roads continues to increase, there will be an increased demand for safety management systems that out-perform their drivers in terms of speed control and collision avoidance through drive-by-wire systems. At the same time there will be a need to transfer much more information to and from moving vehicles, not only for driver information, navigation and entertainment systems, but also for vehicle tracking and road toll applications. The world's limited oil and energy resources will stimulate the development of far more fuel efficient vehicles as well as new alternative energy (battery or fuel-cell powered) vehicles. Nanoelectronics will be at the heart of many of these advances.

Electronic systems for automotive systems have to withstand very harsh environments, including high temperatures, humidity, vibration, fluid contamination and EMC (Electro-Magnetic Compatibility). While these problems have largely been solved for conventional IC-style packaged devices, a whole new set of challenges will have to be faced when these packages also contain integrated sensor, actuator, mechatronic or opto-electronic functions. Some systems, such as collision avoidance radars and engine-assist/traction motor drives, will push the performance limits of current high-volume low-cost semiconductor solutions in terms of frequency capability or power/thermal handling. In addition the critical role in drive-by-wire systems will require extreme reliability, measured in parts per billion instead of today's parts per million. On top of this, the automotive industry imposes special constraints such as parts warranty for up to 20 years and conformance with EU directives.

Security / Safety

Statistics show that we live in a much safer world, yet there is still constant demand for increased safety and security in just about every aspect of our lives, driven by the principle that 'one death is too many'. It reflects itself in public demand for personal emergency and home security systems, and government lead protection from crime and terrorism. Always, however, there is a need for personal protection without restriction of liberty, which means that safety and security systems need to be both reliable and easy to use. It is in this area that Ambient Intelligence's ability to recognise individuals and be responsive to their individual needs will be highly valuable. Nanoelectronics will provide the necessary sensors, computing power and reliability at cost levels that allow safety and security to be built into the fabric of our environment.

Safety and security systems can be divided into two groups. Firstly, low cost personal emergency and home protection systems that are affordable for consumers. Secondly, high-performance high-efficiency systems for applications such as banking, identity card and safety critical systems. To make these systems unobtrusive enough so that we do not end up resenting them they must be small and easy to use. They therefore put high demands on miniaturisation. Yet their requirement to be highly reliable also means that they must be complex and multi-functional so that they make decisions based not on a single parameter but on combinations of parameters (finger-print, voice, iris pattern etc.) This will involve the integration of a wide range of sensors, MEMS/mechatronics and opto-electronic devices. Such devices will also need to communicate reliably by wired and wireless networks, and



Intelligence applied: safety cocoon

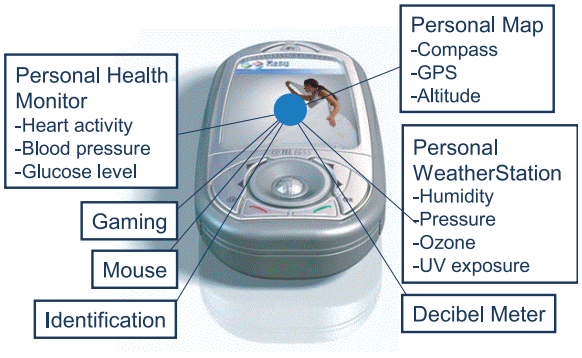
World-wide production of cars is expected to grow to about 70 million units in 2010, compared to the 56 million units produced in 2000. European car manufacturers must continue to be the drivers of innovation in vehicle technology as an important prerequisite for leadership in a market that is of the very highest importance to the European economy and employment. Germany still produces around 25% of world production and about 1/7 of the country's jobs depend on the automotive industry. The European Semiconductor Industry plays a leading role in the development and production of components for the European Automotive market.

In the future, innovation will continue to be based on Electronics and Mechatronics: The Electronic (Nanoelectronic) content will grow to 25% of the whole car production cost in the coming years, leading to an estimated 45 billion euro market for the Automotive Nanoelectronics industry by 2010. Nanoelectronics is one of the most important enabling technologies for innovation in the automotive industry, which will benefit from the ongoing price decline for semiconductor components in new technology generations. As a consequence, car production costs are expected to fall by around 15% by 2010 compared to the year 2000 with respect to the same functional complexity.

they must be made tamper resistant and able to withstand environmental conditions that might affect their performance (radiation, chemical corrosion, shock etc.)

Communication

People are becoming used to having easy access to friends, relations and information services, and more frustrated when that access is not available to them. Making information available anywhere at any time relies on connectivity and communications, increasingly via the use of wireless-based networks (cell-phones, Wi-Fi networks etc.) to meet the 'anywhere' requirement. In future, such communication systems must be even easier to use, even to the point where specific connectivity channels become irrelevant to the user. Information will simply tunnel itself to its destination by whatever communications channels are available. At the same time, the bandwidth of systems will increase dramatically to cope with the increasing amount of data that people want to move around (voice, pictures, video, file transfer etc.) and they will become much more secure against eavesdroppers and hackers.



Intelligence applied: personal comfort

Nanoelectronics will be needed not only to meet the miniaturisation requirements of handheld portable communications devices. It will also be needed to allow much more functionality, in terms of the number of different communication chan-

Although significant progress has been achieved in the past 5 years for safety on the road, injury and property damage due to accidents still remain a major socio-economical challenge for the future. In 2000 the economic loss due to accidents amounted to around 410 billion euro worldwide, about 40% of this being incurred in the EU. As a consequence, the European commission declared its goal to halve the number of people killed due to accidents in the next decade — an important step closer to the ideal figure of 100% safety on the road.

One of the main innovation efforts in the Automotive industry is therefore focused on new 'Active Safety' systems to prevent collisions, subsumed under the title 'driver assistance'. This is based on a 'cocoon of sensors', which detect the surroundings of the car up to a distance of a few 100m. Information from these sensors will be used to inform the driver about critical situations in the traffic, and even to influence the dynamics of the car if the driver is not able to react in time. It has been shown in studies that the probability of an accident can be reduced by up to 65% simply by reducing the driver's reaction time by about 50% with the aid of electronics.

Another important innovation in this area is 'Car-to-car communication' to enable safe-driving interaction between cars on the road. This is especially important where sensors alone are not able to detect all critical traffic situations – for example, cars approaching round curves, overtaking intentions, or unexpected changes in the direction of an oncoming car etc.

For the development of these innovative systems the following enabling technologies are needed:

- A broad spectrum of semiconductor technologies: Bipolar for high sensitivity sensor signals and RF applications, CMOS for computing power and DMOS for actuator drive. These technologies have to be made available in line with the progress of the CMOS mainstream

nels, to be packed inside them. The 'multi-band multi-mode' devices that this will enable will be the key to decoupling communication from specific communication pipes, heralding a whole new era of seamless communications. At the same time, wireless communications channels will move to higher frequencies in order to increase data rates and maximize spectrum usage. This will require the increasing integration of RF MEMS and new RF architectures that allow circuitry to be re-used across many different RF channels and modulation schemes.

As portable communications devices pack more functionality, low-power consumption will become an even more critical requirement. The need to keep devices active for long periods of time between battery re-charges or even autonomous in terms of energy supply, will require the integration of energy scavenging devices that pull and store power from the local environment. At the same time, affordability, reliability and environmental compatibility (disposability, re-cycling and re-use) will be other major drivers.

Education / Entertainment

Content for education and entertainment must not only be accessible anywhere and anytime. It must also be of the right quality and accessible in the right format. Access to similar information will be required in many different locations (at home, in the car, in the street, in hotels etc.) and delivered through a variety of channels (terrestrial, satellite, cable, phone line, wireless, discs etc.). Yet in each location the rendering device for that content, and people's expectations of it, will be different (for example, what is expected from a flat-panel TV set compared to a video-phone). Pre-recorded digital media, such as DVD and HDTV, have increased people's expectations of video quality, yet this video quality will have to be delivered through existing networks.

technologies according to Moore's Law.
- New sensors (MEMS technology, combining mechanics, nanoelectronics and software) for the recognition of different types of object on and beside the road
- New methods and techniques for proving the reliability of these safety critical systems, which are required to have zero failure rates by the Automotive industry
- Automotive-specific Electronic Design Automation tools which are capable of handling the increasing complexity of electronic systems with respect to the required time-to-market for new products
- New assembly and packaging technologies following the size reduction of semiconductor components as a prerequisite for the realisation of highly integrated heterogeneous Systems-in-Package (SiP) solutions.

The societal and economical benefits are easily visible: fewer fatal accidents and injuries, less property damage and assured employment in a growing Automotive Industry.

The need to deliver high quality media through a range of different communications channels while maintaining the required quality will require new developments in multi-format encoder/ decoders, data compression and transmission systems, with media senders (e.g. internet servers) automatically tailoring transmission to the capabilities of the rendering device on which the content will be experiences. Storage and distribution (CD, DVD, digital home networks etc.) will need to be developed that are compatible with the digital rights management requirements of content providers.

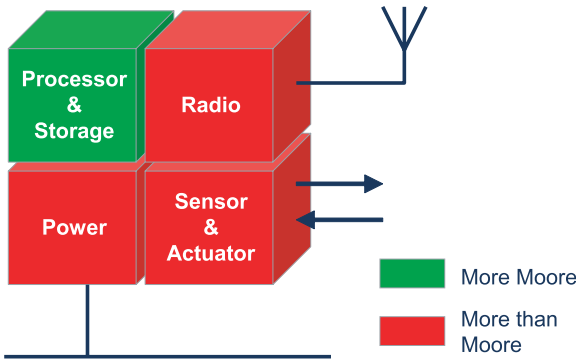
Content generators will require new equipment (for example, HDTV studio equipment and lightweight portable HDTV cameras) to capture content and content providers will need advanced video compression and transmission schemes to distribute it. The demand for users to create their own content will also require significant advances in areas such as image capture (digital cameras, camcorders etc.) image analysis and picture quality improvement at affordable consumer-product prices.

Applications specify technologies

In 1965, Gordon E. Moore postulated a bold theorem that predicted exponential growth in the circuit complexity achievable using wafer-scale semiconductor technology. Through the years, this exponential growth in circuit complexity has become known as Moore's Law. Moore's Law, however, is not a law of nature. It is fundamentally an economic argument which states that the cost of delivering digital functions on silicon wafers – for example, storing one bit of information – can be halved roughly every two years. It is this cost-down enabler that has allowed the microelectronics industry to continuously expand with double-digit growth over the past four decades.

Identifying and tracking the key parameters and technological challenges in the semiconductor industry has become a science in itself, the results of which are published in the International Technology Roadmap for Semiconductors (ITRS). The ITRS is a global forum populated by semiconductor makers, equipment and material manufacturers and suppliers, institutes and universities. The information provided in its annual updates and symposia plays a leading role in determining the world's semiconductor technology agenda.

The two technological developments that have paved the way for Moore's Law are minimum pattern dimensioning (decreasing) and wafer size (increasing). In 1965, manufacturing relied on 25-mm silicon wafers. Now it is 300 mm. At the same time, dimensions of the smallest patterns on these wafers have been shrunk from the size of a lymphocyte (15 micrometer) to that of medium-size viruses (100 nanometer). Today, Moore's Law is the main mechanism behind the development of the 'brain' in nanoelectronic systems, driving increased data storage capacity and computing power in complex high-volume semiconductor products such as stand-alone memories and microprocessors.



Intelligent systems incorporate More Moore and More than Moore

Such 'brains' will be an essential part of Ambient Intelligence systems, but they must also be able to interact with their environment in an intelligent way. As a result, nanoelectronic systems will also need the equivalent of 'ears, eyes, arms and legs'. These eyes, ears, arms and legs will take many forms. They may, for example, take the form of radio communications that allow Ambient Intelligence devices to reach out to other devices in their vicinity, or power supply circuitry that enables them to draw energy AC line supplies or scavenge it from the environment. They will also be needed for non-electrical interactions, such as providing human interface modalities.

'Moore's Law' technologies that have been developed for digital circuits have made it possible to take the first steps towards realizing these additional functions on silicon. However, many of the device structures associated with these functions do not scale with minimum pattern dimensioning in the way that digital circuits do. Radio circuits, for example, need inductors for which the dimensions are determined by the transmission frequency, not by the minimum features size that can be drawn on the chip. Similarly, AC line power circuits are limited by breakdown fields. Non-electrical interaction devices such as loudspeakers and microphones often rely on mechanical phenomena

that occur at millimeter scale in Micro-Electro-Mechanical System (MEMS) devices. Another example of this is the acceleration sensor that triggers the impact airbags in cars.

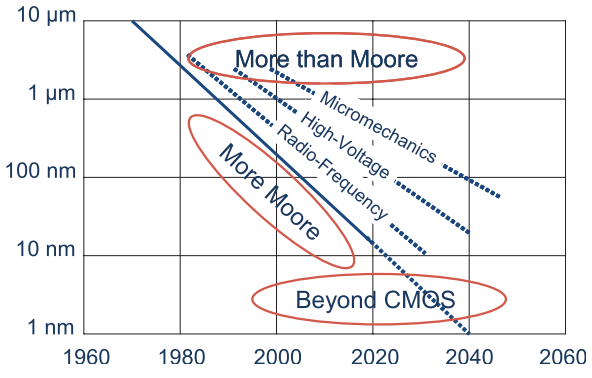
However, integration onto silicon in some shape or form is essential if these non-digital functions are to be made small enough and cheap enough to be built into the everyday items that will be found in Ambient Intelligence environments. Because pattern dimensioning by itself will not be enough to achieve them, innovative alternatives will be needed to cope with ever-increasing market demand and user expectation. From a recognition that these non-digital technologies will evolve along directions other than the straight path of Moore's Law, the domain in which they lie has become known as 'More than Moore'.

Integrated circuits are usually depicted as monolithic blocks of black plastic with metallic lead-outs. This, however, belies packaging complexity. In practice, package specifications are driven by the silicon complexity within them in terms of factors such as silicon die dimensions, number of external connections, heat dissipation and operating frequency, as well as its eventual operating environment in terms of factors such as space constraints, operating temperature and printed circuit board process compatibility.

Packaging can be difficult enough when the package contains the entire system integrated onto a single silicon die – the so-called System-on-Chip (SoC) approach. It becomes even more difficult when multiple die are integrated into a single package to incorporate functions which it is technically difficult or commercially inconvenient to incorporate into a SoC. These multiple die implementations, normally referred to as System-in-Package (SiP) solutions, typically contain a heterogeneous mix of silicon and non-silicon technologies, which further complicates package design.

It is fair to say that SiP is to SoC what More than Moore is to Moore's Law. It provides the design community with an extra dimension to create overall system value. Bringing More than Moore and Moore's Law together in semiconductor products is the battle field of 'Heterogeneous Integration', where nanoscale and microscale technologies meet. A common challenge in More than Moore and Heterogeneous Integration is the apparent absence of functional parameters that scale with pattern size, implying the need for highly innovative solutions other than the shrinking of lithographic dimensions to counter the ongoing market price pressure.

When extrapolating Moore's Law to the year 2020, a point is reached where digital semiconductor circuits as we know them today (transistors and CMOS) will have reached their physical limits. The implications and the alternatives in the 'Beyond CMOS' domain will have to be explored and tested well in advance to allow timely implementation if and when there are needed. Research in the Beyond CMOS domain will involve highly disruptive materials science and device architecture studies.



ENIAC wafer technology roadmap

To bring all above technologies into production, More Moore, More than Moore and Heterogeneous integration, as well as Beyond CMOS, a sound and innovative manufacturing environment is essential, developed in close cooperation with the device technology architects.

European strengths in this area are brought together in the domain 'Equipment and Materials'.

Eventually, of course, all of this has to be designed into products, a process that due to the complexity of today's silicon chips needs to be highly automated. The most complex single silicon chips available today carry as many transistors as there are people on Planet Earth. The level of design automation required therefore involves massive amounts of software.

Research in this area lies in the technology domain 'Design Automation'. It will involve the definition and development of new extensions to electronic design tools that allow designers to implement and verify product designs from system-level specifications right down to physical layout within the time constraints of a short time-to-market and fast ramp-up to volume manufacturing. This is a challenge common to both Nano-electronics and Embedded Systems, which makes Design Automation the glue between the ETPs of ENIAC and ARTEMIS.

Different application domains may differ in the weight given to each of these technologies, but nevertheless they are present in all application domains. Nevertheless, each domain will require strategic direction and roadmaps, together with appropriate consolidated research infrastructures and industry partnerships to achieve its roadmap objectives. Cross-correlated, these roadmaps will allow the early identification of technology issues that stand in the way of achieving the required overall system performance.

Domain 'More Moore'

Tremendous progress in the processing power of integrated circuits (the 'brain' inside electronic devices) made complex smart systems viable. This has been possible through a continuously focussed R&D effort in the 'More Moore' domain now conducted through a network of R&D industrial consortia and internationally recognized Research Institutes. Through the continuous support of public authorities and European programs, the European industry was able to catch up over last 15 years despite strong worldwide competition such that Europe's technological expertise is now on a par with the best in the world.

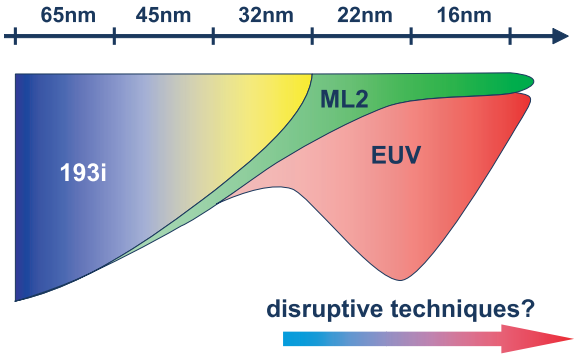
In the 'More Moore' domain, an internationally accepted ITRS roadmap sets the pace, identifying the new 'technology nodes' that will be introduced every 2 to 3 years and highlighting an increasing number of technical challenges that must be addressed. It is not the intent of this document to duplicate the ITRS, but rather to outline the priorities from a European perspective.

Lithography

Lithography is the enabling technology behind the ever-increasing circuit density of integrated circuits (ICs). Europe has a major lead in this field through dominant Equipment & Material suppliers, Research Institutes and advanced Pilot Lines, putting it in the position of driving the associated roadmap.

193-nm optical lithography with immersion and other technology enhancements will prevail for some time to come and should be able to address the 45-nm and probably the 32-nm CMOS nodes. This will be the focus of short-term R&D into lithography in Europe through existing Institutes and Consortia. There are, however, major issues still to be solved in terms of tools (especially high Numeric Aperture durable optics and overlays) and process effects (polarization effects, high-n fluids, resist-liquid interaction, resist limits, defectivity, etc.).

In addition to the need for tightened specifications of the masks (for example, birefringence of the blank), stronger interaction is needed between designers, process engineers and EDA providers in order to relax the lithographic constraint of printing features 'as-designed' onto the wafer. Research work into 'Design for Manufacturability' should provide ways of tackling the problem of escalating mask costs, for example, through applying Optical Proximity Correction only to functionally critical patterns or through the generation of more regular layouts.



Advanced ithography roadmap

The need for Extreme Ultra-Violet (EUV) lithography is not now expected until the 32-nm CMOS node or beyond. This will not only involve solving currently known challenges such as high-power UV source reliability; optical quality, lifetime and contamination; defect-free mask production and mask handling. It will involve solutions to even more challenging technologies, such as Resolution Enhancement Techniques for the 22-nm node and high numerical aperture optics for the 16-nm node). Strong cooperative programs are on-going in Europe which should maintain Europe at the forefront of optical lithography.

The increasing cost and complexity of masks emphasises the need for MaskLess Lithography (ML2) technologies, especially for low volume and short lifetime products. Presently these techniques either suffer from a very low throughput (for example, current e-beam lithography) and/or being still in their infancy. On the other hand, Europe is a region that has significant activity in this field and where ML2 has been tested in manufacturing lines. It therefore represents a major opportunity for Europe to take the lead in bringing ML2 technology to industrial maturity.

Other disruptive technologies such as 'nano-imprint' may find it difficult to displace optical lithography due to major issues (for example, nano-imprint's 1:1 template, overlay correction, etc.) and will initially only address niche applications. There is, however, a clear need for upstream research programs in order to clarify the potential and key issues of these techniques.

Underlying all these techniques, a robust resist technology is also needed. Roadblocks (for example, resolution, line edge roughness and sensitivity) have to be assessed through a combination of in-depth understanding through scientific research and industrial validation. The same applies for Technology Computer-Aided Design (TCAD), where Europe is already leading, and mask manufacturing where there is already significant expertise in Europe.

Priorities

- Develop technology and infrastructures in order to extend immersion lithography to 45 nm and 32 nm
- Develop a technology and infrastructure for EUV for below 32 nm
- Develop strong infrastructures for resist development and understanding of the limiting mechanisms
- Develop ML2 lithography for early development/ prototyping/ low volume production
- Clarify the importance/potential of imprint and other non-evolutionary lithography strategies through fundamental research programs

Logic technologies

The basic information processing unit in today's digital ICs is the CMOS gate. Although its contin-

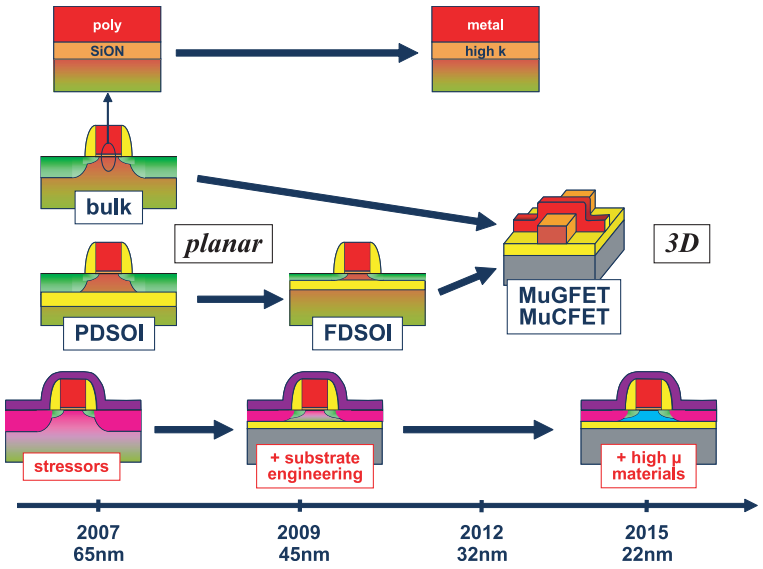
uous size reduction has delivered enhanced performance for decades in terms of speed, power consumption, reliability and cost per function, further progress is needed to tackle more complex optimisations. The diversity of the options to be explored is at the same time an opportunity for innovation and a challenge.

As the critical dimensions of the transistors that make up these gates are scaled down, leakage current and the associated static power consumption of the transistor becomes a major issue. Ultra-thin Silicon OxyNitride (SiON) gate dielectric suffers from a significant tunnel leakage current and no alternative material such as a 'high-k' dielectric has so far been brought to production-worthy maturity. At the same time the electrostatic control of the gate is more challenging at low dimensions. This means that more sophisticated transistor architectures using three-dimensional structures, such as multiple gate FETs (MuGFETs) or multiple channel FETs (MuCFETs), will be needed in the future. However, the process complexity needed to fabricate these devices has so far prevented their early introduction into manufacturing. The 32-nm node will probably be the entry point for these disruptive technologies.

On the other hand, when it comes to enhancing device speed, many approaches are already approaching maturity. In the shorter term, this is being achieved by inducing stress in the conductive channel of the transistor. In the longer term, it may be achieved by replacing silicon channels with more conductive channel materials such as Germanium (Ge) or III-V compounds.

Gradual integrating of these innovations into manufacturing, together with co-design of engineered substrates, material stacks and devices, will enhance the present bulk silicon or Silicon-On-Insulator (SOI) planar transistor, allowing a steady increase in overall performance.

However, inter-connecting all the gates in an integrated circuit remains a major issue. Although transistor performance will continue increasing, the performance of the interconnection network is not expected to match this progress. The effective resistivity of copper i interconnects increases at small dimensions and the dielectric constant of the insulating film below and between the interconnect layers doesn't scale much (even with so-called 'low-k' materials). As a result signal integrity in the interconnect is becoming a major issue.



Simplified transistor roadmap

Strong cooperation between the technology and design communities will definitely be needed to overcome the future limitations of Cu/low-k interconnection networks. Long-term innovations such as air-gap dielectrics and 3-D interconnects will require major developments, while disruptive concepts are unlikely to totally replace the Cu/low-k stack.

Europe is well positioned to handle the challenge of advanced logic processes. It has leading applied research consortia and institutes driving the development of new semiconductor devices and new front-end and back-end processes. It has strong academic expertise in specialized areas, especially in materials, TCAD, and electrical and structural characterization.

On the other hand, insufficient and scattered academic resources are linked to medium-term evolution of the CMOS roadmap. Most academic institutions focus more on exploratory research 'Beyond CMOS'. Provided there is greater efficiency in the link between academia and industrial research, the multicultural expertise, diversity of approaches and cooperation between R&D teams in Europe may become key assets in maintaining its worldwide competitiveness in innovation and industrial leadership.

Priorities

- Develop co-engineered substrates – materials – devices
- Develop technology and devices for high k dielectrics and metal gates for 32nm node
- Develop technology and devices for 3-dimensional structures (multiple gates and channels) for 32nm node
- Develop physical understanding of the limits of the transistors, e.g. transport physical mechanism, device matching, impact of atomic level statistical fluctuations
- Assess limits of the low k/ Cu interconnect scheme & develop innovative solutions (air gap, 3D)
- Enhance design – process synergy

Dynamic Random Access Memories

Memories often consume most of the silicon area in complex ICs. The driving parameters for advanced memories are primarily integration density, which translates into an aggressive scaling path, followed by non-volatility, speed and energy consumption.

Stand-alone or embedded in ICs, Dynamic Random Access Memories (DRAM) targets very high storage capacity together with reasonable retention. Scaling the dimensions in order to increase storage density translates into very demanding lithography, extremely high aspect-ratios that push deposition and etching to their limits, the need for new materials for the capacitors and ultra low-leakage access transistors. This last factor is the main driver behind the development of 3-D transistor structures for introduction one node in advance of that for logic devices). The question is whether or not the increasing process complexity will reduce the productivity gain expected from pure scaling (30% bit cost reduction per year). This is why the introduction of 450-mm diameter wafers will be required in the longer term.

Europe has a strong development and manufacturing base and can rely on the flexibility of R&D Institutes to develop and integrate new materials. Integration of new materials will especially be needed for the DRAM capacitor, where reliable high-k dielectrics with low equivalent thickness will be needed and where the transition from a Metal-Insulator-Semiconductor to a Metal-Insulator-Metal capacitor is expected at the 45-nm node.

Priorities

- Development of new materials for the capacitor
- Develop new memory structures for beyond 30-nm (e.g. interleaved capacitor DRAM)
- Introduction of 450-mm wafers

Non-Volatile Memories

Non-Volatile Memories (NVM) are important features in many products and the current mainstream technology for implementing them is Flash, both for stand-alone NVM devices for mass storage or NVM embedded in SoCs. Europe has strong research centres and universities with good expertise in NVM and the European semiconductor industry is also strongly involved in NVM products. However, non-European companies drive technology leadership in NVM.

From a technology perspective, scaling current Flash processes will be the preferred route for as long as new materials and architectures are not mandatory. High-k materials are expected to be introduced firstly as an inter-poly dielectric at the 32-nm node, while tunnel oxide could be replaced by a crested barrier at the 22-nm level. Coupling between cells is a major issue in NAND Flash memory arrays and will push the introduction of low-k dielectric from the 45-nm node onwards. Later on, probably at the 22-nm node, both NAND and NOR Flash will require three-dimensional cell structures.

Emerging 'unified' memories having the performance of SRAM and the density of DRAM together with non-volatility are a constant quest. Some concepts, such as Ferro-Electric RAM, are already in production while others such as Magnetic RAM may soon be. With all these technologies, however, scaling to smaller geometries seems to be problematic in the long term. In this respect, Phase-Change RAM seems to offer more promise. The introduction of inherently bi-stable materials (e.g. molecules) as the base element for high density universal memories is still at the 'proof of concept' stage. For these approaches, research is needed both in terms of materials science and architectural exploration in order to demonstrate their potential to surpass the expected performance of scaled Flash devices.

Priorities (short term/ Flash)

- New materials: high-k as interpoly, discrete traps layer for charge storage, low-k
- 3D cell structure exploration

Priorities (long term/ 'unified' memories)

- Research on new concept/ material, new memory cell/array architectures
- Competitive with scaled flash memories (cell size, reliability, CMOS compatibility, scalability, etc.)

Transverse technologies

'Low power' is a key word, especially for products developed in Europe. In most cases, it is unreasonable to expect breakthroughs from a pure technology standpoint or from a pure design methodology. Enhanced synergy between application, design, device and process development will be a key asset for those organizations attempting to find an efficient way to achieve low-power systems.

The scientific understanding of process steps (e.g. clean, etch, CMP, etc.) is needed to complement the pragmatic approach of process engineering especially as we enter the nanometer regime.

The development of structural metrology (accurate 3D measurement of different patterns) as well as of structural off-line characterization (including morphological, physical and chemical analysis of 3D nm-sized structures made of complex material stacks) is a challenging research field which may boost or hinder technological developments.

A physical understanding of the electrical behaviour of functional structures (including reliability issues) and its abstraction into an accurate compact model is mandatory for designing complex circuits. Europe has a strong expertise in these fields which should be maintained in the nano-era.

Many cooperative programs and the strong commitment of a few leading Institutes has brought European TCAD expertise to the highest level.

Strong support is needed to maintain this position for the future technologies.

Manufacturing science is a key research area that may help to preserve a manufacturing base in Europe. This field is usually not a priority for academia – industry cooperation and may gain from a stronger synergy.

Conclusions

Europe has good potential to bring solutions to the technical challenges in the 'More Moore' domain to ensure steady progress. As technical conclusions Europe should maintain the leadership in lithography, reinforce the material research oriented towards nanoelectronics, favour the technology – design – application synergy, and maintain its excellence in specific domains (e.g. compact models, TCAD, etc.).

However, in order to reinforce the efficiency of the whole R&D 'supply chain' from academia to applied research institutes and industry, many specific facts from the 'More Moore' domain need to be highlighted:

- Most R&D is driven by the industry (especially through the ITRS)
- It is short- to medium-term time-driven R&D
- Final process integration is cost/capital-expenditure intensive. R&D using 300-mm silicon wafers is beyond the financial capacity of individual organizations or countries. It needs strong support at the European level to complement national and/or industrial initiatives
- For early technology assessment, there is a need for flexible low-cost pilot lines combined with a strong scientific expertise, which can be achieved at the national level
- Manufacturing awareness on the part of researchers is definitely needed to focus their work on fields that have the potential for introduction into a volume production line

Taking these facts into account we recommend for the future 7th Framework Program to:

- Acknowledge the advantages of creative competition as long as the resources exist
- Focus funding on a few state-of-the-art 300-mm infrastructures in a few locations (European competence clusters)
- Give guidance and stimulate networks of academic excellence that have access to these infrastructures
- Encourage additional small, low-cost, flexible infrastructures for added-value exploratory research
- Support academia in making nanoelectronics more attractive to young people

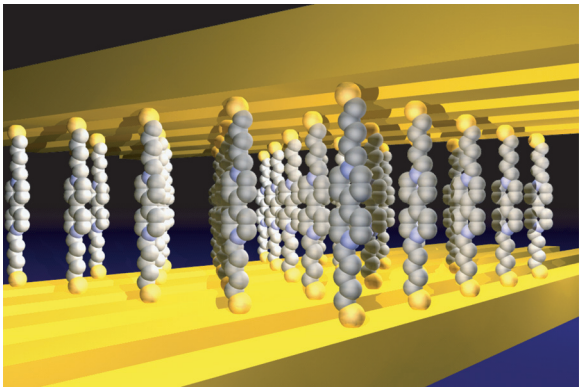
Domain 'Beyond CMOS'

For many years, experts have been discussing when classical CMOS would come to an end and what would replace it. Actually, we believe that when classical CMOS does not work on its own any more, it will at first be complemented with non-classical elements. Only later on will technologies 'Beyond CMOS' be introduced.

The entry point for 'Beyond CMOS' technologies into production may be around the year 2020. However, in view of the long time needed to turn first ideas into production processes, an early start to activity in this area is needed. On the following pages a strategic approach will be outlined, starting with the current state of the art and proposed objectives, highlighting examples of key topics that need to be addressed up until the year 2013, and then examining the outlook beyond 2013. Finally, an assessment of the strategic relevance, timing and required effort is presented.

We are approaching the CMOS scaling limit because we are reaching a point where an increase in power consumption coincides with an insufficient increase in operating speed. The disproportionately small increase in operating speed is caused by a decrease in channel mobility and an increase in the interconnection resistance for smaller process geometries. The power consumption is largely due to increased leakage currents, short channel effects, source drain tunnelling and p/n junction tunnelling. At the same time, the increasing significance of defects and the high level of complexity in both lithography and design have resulted in manufacturing costs rising dramatically. Even without taking into account physical limits, all these effects combine to push us closer to a point where we reach the limit of CMOS scaling.

There are a large number of different 'Beyond CMOS' options – but all are in an embryonic pre-industrial phase, without a stringent strategy to guide their development. Because 'Beyond CMOS'



Nanowires

is still rather far away and because there are so many possible but non-mature solutions, the main objective of this part of the SRA is to enable effective decision making and to develop a methodology for bringing the chosen technology options into production. The Strategic Research Agenda for Technologies Beyond CMOS will describe the necessary steps to bring Beyond CMOS to industrial maturity at the right time (probably even after the year 2020), with the right performance and cost, while also taking into account safety, health and environmental issues.

In order to reach these targets, the following steps have to be performed

- Right selection of possible emerging technologies
- Identification of the required preparatory work
- Development of a strategic work-plan for evaluation, preparation and implementation of the emerging technologies including appropriate design methodologies

Topics until 2013

Unfortunately, the overview of potentially important topics reads rather like a shopping list. Some of the most debated options, excluding the non-classical CMOS options, are briefly listed below.

Architecture:

- Defect tolerant
- Biologically inspired (Molecular computing)
- Parallel processing

An important prerequisite is the availability of interconnects that are scalable and compatible with Beyond CMOS architectures

Logic devices and memory concepts:
- Metallic nanowire transistor
- Molecular / organic transistor
- Direct tunnelling devices
- Resistance and phase change memory

Materials:
- Interconnects:
  Optical interconnect
  RF interconnect
  Nanotube interconnect
  Molecular interconnect

- Channels:
  Silicon nanowires
  III–V compounds
  Molecular nanowires

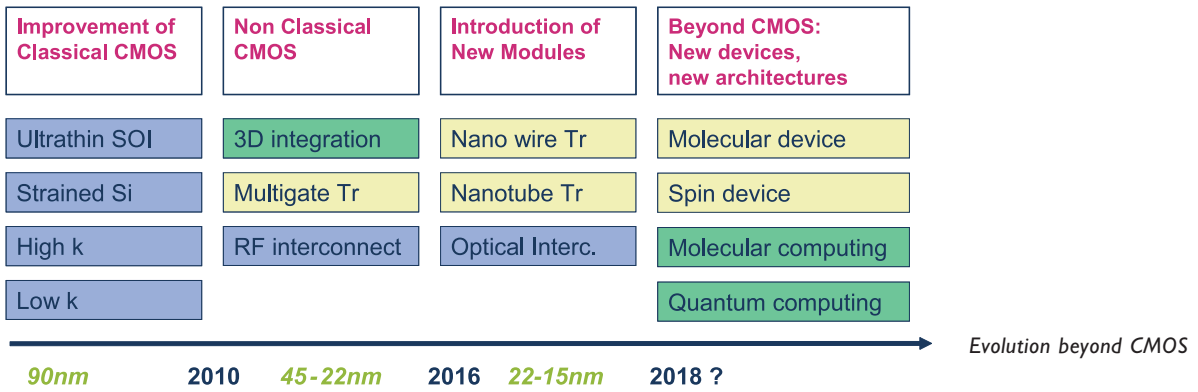
In order to compensate for the practical difficulties caused by the extremely high complexity and integration level of all of Beyond CMOS devices, they generally have to be defect-tolerant, and parallel and/or hybrid design has to be applied.

The strategic relevance of the different Beyond CMOS options/modules can be derived from the need to replace or to complement classical solutions that no longer have the required performance or are too complex/expensive for industrial application. In a non-complete but systematic way this is visualised in the below picture.

However, a selection still has to be made from the large number of options. As a clearly defined strategic selection of the different options is not yet possible, a 'lock gates' channel for innovation is proposed as shown in the next figure.

The main principles of this proposed 'lock gates' channel are that it represents a non-stop evaluation process with incremental evaluation and an iterative process at each stage. The process should be technology driven but subject to constant societal needs analysis. It should also be an open process that allows the participation of start-ups, spin-offs and SMEs as innovation boosters.
The different steps of the process can be characterised in the following way.

Lock Gate A:
Upstream to applied research
Proof of concept level - possible on lab-scale, using a few small wafers
- Clear advantage compared to CMOS demonstrated or foreseen
- Address a bottle neck issue
- 1 or 2 order of magnitude gain
- Multi-function capability



Lock gate B:
Applied research to industrial research
Component level - needs some hundreds of 200 / 300 mm wafers
- Information propagation
- Isolation between output and input
- Signal restoration (gain, non linearity)
- High fan-out / drivability
- Tolerance to fault, fluctuations, noise
- Room temperature operation
- Scalability

System level
- Integrated function demonstration
- Clear path for system integration
- Impact of health and environment

Lock gate C:
Industrial research to industrial development
Demonstrator level - needs many hundreds of 300 mm wafers
- Tools available
- Mass production at affordable cost and yield
- Capability of reaching critical mass
- Resources
- Research intensity and depth
- Capability to combine peripheral competencies
- ESH (Environment, Safety and Health) compatible

Lock gate D
lindustrial research to product
Product level - needs thousands of 300 / 450 mm wafers
- Final assessment of cost
- Final assessment of throughput
- Final assessment of time to market

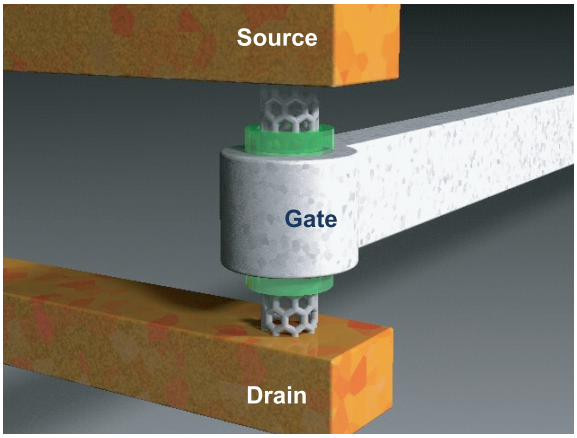
Topics beyond 2013

After the year 2013, the industry will request even more advanced devices that are at least partially out of the reach of current predictions. Structure size, complexity and functionality will need requirements specifications to be fulfilled at moderate costs, which may need completely new concepts. As for the nearer future, some examples of the most discussed solutions are listed below.

Architecture:
- Cellular Array
- Quantum computing

Devices:
- Nanotube transistors
- Spin transistors
- Single electron transistor
- Single electron memory
- Molecular memory
- Nanotube mechanical switch

Materials:
- By self assembling wiring processes for sub-litho structures
- Superconducting materials (at room temperature or using solid-state cooling)
- Quantum dot



Nanotube transistor

Conclusions

For industry, 2013 is too far away for it to put sufficient effort into the evaluation of the technology options that will be needed beyond that date. However, it is essential that Europe is prepared so that it does not miss opportunities or choose totally impractical options.

A system of collecting the necessary information therefore has to be devised that enables Europe wide, possibly a world-wide, survey of emerging

technologies to be started within the next three years (Industrial Monitoring). Possible analyses could include cartography with respect to technical parameters, environments or other relevant arguments in favour or against new solutions. This systematic assessment should be supported by a parameter matrix that shows potential and risk described in terms of technical and economic parameters.

The technology platform ENIAC offers a unique opportunity to trigger the collaborative effort required. It will foster strong links between Beyond CMOS and the scientific community, which will help to combine competencies from industry and academic research.

To support the assessment procedure we urgently need to improve our prediction/simulation instruments in order to accurately predict and optimize the molecular features and electrical behaviour of the devices; to optimize, understand and improve the self-assembled organization and the growth and control of totally new compounds such as Carbon Nano-Tubes.

To ensure long-term success we need to do much more today in Physical Chemistry and Material Science and also much more in Computational /Quantum Chemistry and Physics. Once again, this will demand a concrete effort in fostering co-operation between industry and academic research. Concentration on one discipline must be replaced by multidisciplinary research where large scientific networks exploit new opportunities.

Domain 'More than Moore'

In recent years, we have witnessed the emergence of an increasingly diverse area of microelectronics that goes beyond the confines of Moore's law into the area of More than Moore. A typical example is the on-going integration of passive components such as inductors, capacitors and resistors onto silicon in order to meet the integration requirements of today's multi-band multi-mode mobile phones.

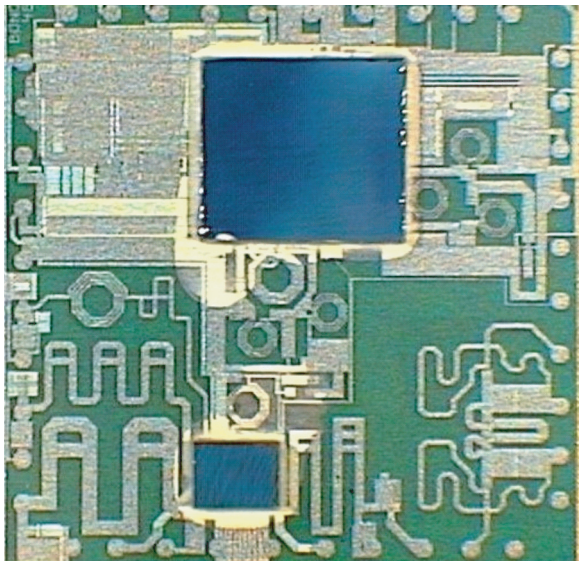
In addition to the dedicated non-CMOS semiconductor process technologies needed to implement high-voltage, low power, analog, and radio frequency devices, new semiconductor technologies are needed to realize mechanical, thermal, acoustic, chemical, fluidic and optical functions. Nano- and bio-technology are also around the corner, both of which will require new wafer-processing technologies. Heterogeneous integration will then be the key enabler for integrating these diverse semiconductor technologies into multi-functional products. In the world of Ambient Intelligence it will eventually lead to a direct interface into the environment or even the human body.

Radio-frequency

Many of today's electronic systems utilize radio-frequency (RF) circuits to transmit data internally or externally. Typical RF application include wireless communication, wire-line communication and short-range connectivity and mobility.

Mobile RF applications range from GSM, 3G and 4G cellular communications, to Wi-Fi access and 60 GHz wireless LANs, providing point-to-point and multi-point connections for voice and data, video distribution and internet access. Convergence means that many products are now multi-band and multimode, not only using RF communications for voice and data transmission but also for localization and navigation. As a result, many feature multiple air interfaces and advanced antennae systems.

The higher bandwidth demanded by voice, data, music, image, video transmission requires higher frequency wireless links, while the need for handheld mobile devices to operate from smaller battery packs demands low-power wireless operation. This requires innovation in the analog RF front-end section (active and passive functions) as well as in the digital section to achieve higher processing speed and computing power for lower power consumption.



Passive integration on silicon: DECT full radio module

Most of these RF devices need the support of a wireless infrastructure such as the basestation network for mobile phones or the transmitter network for digital terrestrial TV. With the worldwide expansion of mobile phone networks and wireless internet access networks there is very rapid growth in the basestation market. Because these basestations have to simultaneously support a large number of transmission channels, they require high bandwidth tuneable RF power amplifiers with very high linearity and higher operating efficiencies. The main challenge here is to achieve reliable, robust and cost effective technologies (long lifetime) for use in RF front-end circuits for mobile communication basestations and wireless point-to-point and multipoint broadcast systems.

Many of these local infrastructures then link into global infrastructures that carry data vast distances via satellite, microwave or optical fiber networks. These global networks require extremely high performance (high frequency) technologies, the main challenges being high-speed circuits and technologies at 40 and 80 GHz. The vast number of multiplexers in these systems also means that power consumption per multiplexer (< 5 Watt) is a critical design requirement.

There is also a local networking (access) requirement for fast broadband access in offices and for home applications via standard copper (telephone) wires. In practice this will mean a mixture of wireline and wireless interfaces operating at various levels. The main challenge here is the reuse of standard technologies in volume production enabled by integration of new devices (such as LDMOS transistors) to enhance driving capabilities at low power. There are also proposals to transmit data via standard copper power lines (AC line power cables), where the main challenge will be to extend the bandwidth and frequency for data transmission.

Higher frequency (microwave) applications also include short-range collision avoidance and road-safety systems in vehicles (24, 77, 110 GHz) radars and imaging devices for aircraft take-off and landing safety systems and imaging systems for access control, the detection of metallic and non-metallic materials (explosives, ceramic weapons). This will involve the development of high-speed spatial resolution short and medium range sensors, radars and imaging systems operating at frequencies up to 1 THz. The main challenges here are achieving the required frequency and bandwidth and reducing sensitivity to effects such as humidity, temperature and mechanical impact.

Priorities

- Increase process speed in terms of frequency

to enable more computing power and/or running systems at higher frequencies for better precision
- Increase power efficiency and reduce power consumption (e.g. leakage currents) to achieve longer standby times and less power dissipation
- Decrease noise and spurious levels to allow higher RF integration in standard CMOS
- Improve process/device tunability to meet the need of broader spectrum of applications
- Develop on-chip and chip-to-chip connections (e.g. transmission lines) with reduced losses for high speed applications and 3 D packaging and 3 D interconnect techniques
- Reduce form factor in RF architectures
- Carry out implementation studies into simplified antenna systems
- Development of high performance, small size, low cost passive functions e.g. high-Q inductors, tight tolerance capacitors, high density capacitors, low loss switches, RF filters, tunable capacitors, RF MEMS
- Optimise Q-factor (quality) for all components and reduce substrate losses
- Develop technologies for integration of RF building blocks (passive and active) into SiP modules
- Develop re-configurable RF circuits
- Develop models of components and devices for frequencies up to 60 GHz and above.
- Improve CMOS and BiCMOS technologies for higher integration levels
- Develop 'dirty RF' with digital compensation/calibration for 'Digital Radio'
- Evaluate high-efficiency RF MEMS and filters
- Optimise GaN and other III/V technologies for RF Power applications
- Improve technologies for multiplexing and interconnectivity with optical-electronics
- Extend III/IV and SiGe technologies to1 THz
- Optimise antennae architectures on chip (e.g. multi-beam)

High-voltage and power

High-voltage (HV) can be defined as any voltage higher than that used in the classical digital I/Os within state-of–the-art semiconductor processes, i.e., starting at 3.3 or 5 volt. HV interfaces and functions are important parts of most (small) systems, usually as part of an input/output (IO) system that interfaces the system to the real world. They are usually needed when the I/O device requires a high power or high voltage drive (e.g. mechanical actuators or LCD displays), or when high-voltage capability is required in protection circuitry that allows sensitive electronic circuits to be used in harsh environments (e.g. automotive systems). High voltage capabilities are also required in power management, power conversion and power distribution circuits.

Power management solutions are required to drive low voltage CMOS circuitry from battery or AC-line power sources in a wide range of consumer products. Automotive systems need to drive mechanical actuators such as in fuel injection systems, solenoid drivers, starter engines and electric windows, but are also increasingly typified by low-voltage electronic systems in body control and drive-by-wire systems that need protection from voltage spikes. The emergence of engine-assist and electric vehicle technology is moving car battery systems from to circuitry capable of handling 200 V. High voltage capabilities are also needed in solid-sate lighting systems and battery chargers.

Power generation and distribution systems include new portable energy sources such as micro-fuel cells and micro-batteries, high power DC-to-AC converters (e.g for solar cells) and decentralised and regenerative energy supplies (wind power plants, fuel cells, micro-turbine, solar panels etc.)

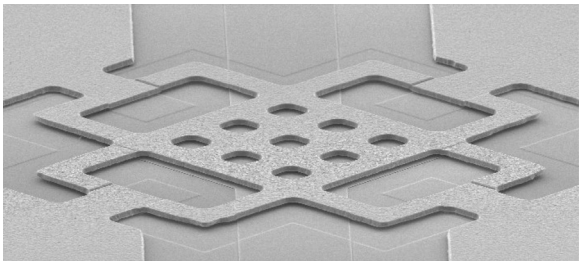
Priorities

- Reduction of transistor on-state resistance to reduce power losses and breakdown voltage

- Improve switching performance for higher switching frequencies
- Improve electrical robustness (e.g. reverse voltage, ESD etc.) and operating temperature range
- Improve integration density when combined within a CMOS environment via advanced interfaces between silicon and package
- Reduce the resistance of HV MOSFETs in silicon to bridge the gap with GaN/SiC technologies
- Develop high-voltage/high-current interconnect architecture with thick Cu metallisation
- Develop new isolation technologies, such as selective SOI, to allow more flexible integration of HV devices with CMOS, lower leakage, and higher operating frequency
- Develop energy scavenging systems for autonomous systems
- Develop advanced thermal management and cooling
- Develop high-level Sip for solid-state lighting

Sensors and actuators

Sensors and actuators play an essential role as the interface between electronic systems and the user/environment, particularly in Ambient Intelligence environments. The majority of the sensors in use today are stand-alone devices measuring parameters such as pressure, magnetic field strength rotational speed or acceleration / tilt. Most of these physical parameters are measured in an indirect way. For example, rotational speed is often measured using magnetic field variations induced by a toothed wheel. Integration into larger systems has only just begun and new functionalities are emerging.



RFMEMS band switch

Sensors and actuators are employed in a vast range of applications, each having its own application requirements. Typical applications include audio systems, tyre pressure monitoring, personal navigation, positioning, pre-crash detection, distance measurement, 3D-imaging using ultrasound, bio-chemical detection, and human interface devices (touch pads, finger print).

Different competing sensor technologies may coexist, often pursued by different players with proprietary solutions, and often implemented as dedicated system solutions. Added value in the sensor market is at the module or system level, which is highlighted by the trend towards smarter, more highly integrated, miniatuturized and hence more compact sensor systems and modules.

Priorities

- Develop new, functional and compatible materials
- Develop application oriented technology platform, system architectures and re-use technologies
- Develop cost effective packaging solutions for sensor/actuator, MEMS and NEMS (nano-scale MEMS) applications
- Improve methods and practices of design ing for manufacturability, reliability and testability
- Develop and implement integrated multi-scale and multi-process modeling, simula tion, optimisation and design tools and methods in product creation process
- Develop and apply novel nanotechnolo gies, such as nanowires and nanotubes, for sensors and actuators

Bio-chips and fluidics

Micro- and nano-technologies will provide powerful devices for biological applications. For more than ten years, DNA micro-arrays have revolutionized genetic analysis in life science laboratories. However, it is widely accepted that beyond this breakthrough there is real potential to create

totally new analytical tools for biological applications. Many of these will generate mass markets in areas such as in-vitro diagnostics and healthcare, drugs and drug delivery systems, environment control (air, water, soil), agriculture and food, defence and civil security.

Cell interacting with nanotube structure

A wide range of sensor types will be required, such as bio-chemical sensors, spectroscopic sensors, Ion-Sensitive Field Effect Transistors and media sensors for detecting parameters such as CO_2 levels, fuel and oil condition, ozone concentrations, particulate matter, hydrocarbons, gas, etc.)

Typical applications will include measuring devices for clinical 'observation' such as blood pressure monitoring (sphygmomanometer), volume of inspired/expired air (spirometer), oxygen consumption (ergospirometer) and heart (ECG) and brain (EEG) function; devices for minimally invasive surgery and drug delivery; bio-hazard detection and DNA/protein assays. Applications such as DNA/protein assaying in the form of a lab-on-a-chip will also require the development of micro-fluidic systems such as micro-pumps, valves and mixers.

Priorities

- Develop fully integrated microsystems to perform a complete molecular diagnosis, including advanced micro-fluidic technologies to control the move of ultra-small volumes
- Improve biological detection and signal processing methods (nanowire based sensors?)
- Control of physicochemical properties of solid surfaces (for example, through thermal, optical, or electrical phenomena)
- Achieve cost effective and robust bio-compatible materials and processes

Conclusions

The success of More than Moore depends on not only the availability of the required technologies and competencies, but also on the existence of industrial visions, strategies and business models that allow optimisation of entire value chains to fit the characteristics and needs of specific applications. It is worth mentioning that for all the technology building blocks of More than Moore, cost and time-to-market are two dominating factors that will ultimately determine both the relevancy and priority of proposed research subjects. The following issues deserve more attention for More than Moore development:

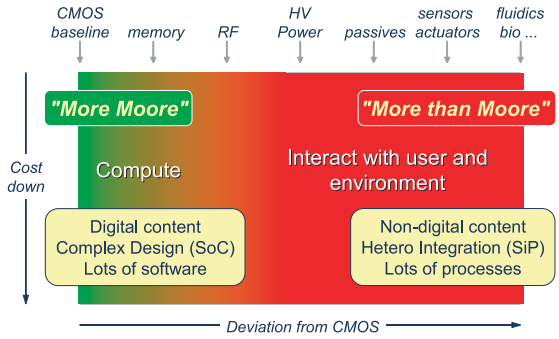
Several elements need to be considered in defining new More than Moore business models. Firstly, with more functions being integrated into a single (sub-) system, partitioning in the value chain changes both in terms of the involvement of the different parties involved and in terms of their profitability. This may lead to changes in the industrial landscape and competitive balance.

Secondly, new and quantitatively reliable cost models have to be developed. Currently some of the less well developed More than Moore technologies have un-clarified cost consequences. Even for More than Moore technologies that are close to being adopted, the cost of heterogeneous integration is not always well-defined. This is the case, for example, with the 'known-good-die' requirement.

Supply chain management is another important

element, because of the immaturity of many More than Moore markets and little consolidation in the number of industrial players involved. The winning business models will be those that integrate and optimize all these important, interlinked, sometimes controversial, elements.

The success of Moore's law has been enabled by an excellent ecosystem consisting of public awareness; the availability of resources (man-power, materials, finance, etc.); the existence of R&D and manufacturing and supply chain infrastructures; and market maturity. To create effective and efficient ecosystems in the More than Moore business, partnerships will be essential.



More than Moore and Heterogeneous Integration are connected

As an initial step, partnerships in the electronics sector should be further strengthened. In the past decade, much of the electronic industry has abandoned the vertical operation model and focused on its core business. More than ever before, they are now interlinked with each other in the industrial value chain. Collaboration on content is common place, despite business competition between them intensifying. For the More than Moore business, there is a clear need to standardise and commoditise some of the required technologies and designs in order to enable product manufacturing to be quickly ramped up to an economic scale. This can only be achieved by establishing structured cooperation within the electronics sector.

As a second step, partnership between electronic industries and non-electronic sectors (such as automotive, healthcare, etc.) will be vital. For More than Moore related technology and new product development, it is important to know the market requirements and trends in order to master the required application knowledge, share the R&D costs and gain access to markets beyond the traditional operating scope of electronic industries. By joining forces with application sectors, it will not only be possible to enlarge existing markets (for example, automotive and lighting). It will also be possible to drive the emergence and growth of new markets (for example, health care and personal wellness).

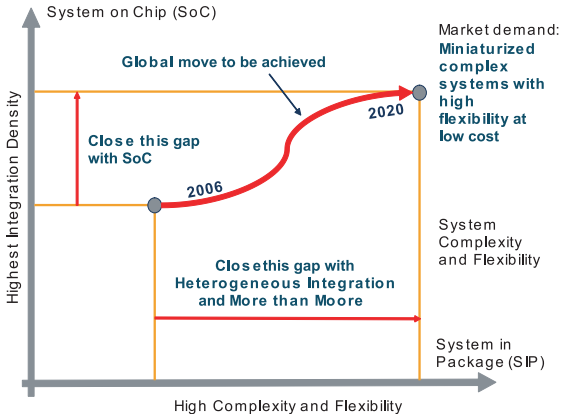
As a final step, partnership between industries and academia should be better structured and intensified. The associated benefits are twofold. Firstly, it will help to speed up the creation of fundamental knowledge in order to counter the fact that the gap between industrial requirements in the More than Moore business and the availability of fundamental research is getting larger. As a result, trial-and-error methodologies are still daily practice. Collaboration between industry and academia will improve the efficiency and industrial relevance of fundamental research. Secondly, it will greatly increase the success rate of innovation. In the past two decades, the academic community has invested a lot of effort in working on More than Moore related technologies and even in product creation (for example, sensors and MEMS). But many times, the industrialization of their R&D results has not been given sufficient attention and effort. This has hampered the beneficial commercialisation and economic impact of some excellent R&D results.

Although high-technology start-up companies have to some extent filled part of the gap, it is difficult to push More than Moore technologies and products into mass consumer markets without the leading electronic industries committing their resource and capabilities. Teaming up with acade-

mia from the beginning of the technology / product creation processes will help to ensure that this happens.

Domain 'Heterogeneous Integration'

The future of nanoelectronics will see a combination of 'More Moore' and 'More than Moore', of 'System-on-Chip' and 'System-in-Package'. With a SiP solution, the application benefits from a comparable level of miniaturization to that achievable with a SoC, but it also benefits from having each part of the system fabricated in an optimum process technology. SiP solutions will typically contain SoC solutions ('More Moore' solutions) but combine these with other devices that provide an optimised performance, improved time-to-market and overall value for money.



Closing the gap with SoC and SiP

It is Heterogeneous Integration that will not only bring all these components together into one package but also provide an interface to the application environment. It therefore represents the glue between the world of nanoelectronic devices and systems that humans can interact with. Heterogeneous Integration has to ensure the integration of components based on different technologies and materials. For example, an ultra-miniature single-package bio-sensor could contain photonic components for detection, RF components (using InP or GaAs) for communication and energy scavenging or energy storage components (thermoelectrics, fuel cells, thin film batteries) for

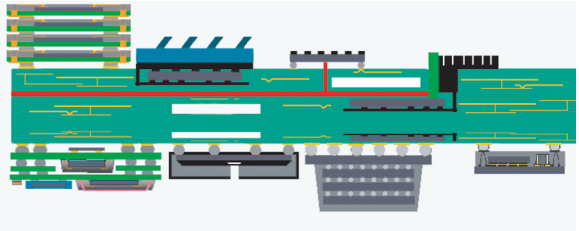
power. And because the reliability of such systems will be of increasing importance, future heterogeneous integration technologies will have to achieve failure rates measured in parts per billion rather than today's parts per million.

The present status of system integration is still dominated by single-chip packaging, with the few stacked-die SiP solutions being implemented mainly using wire bonding. The most advanced substrate boards are High Density Interconnect multilayer boards. Unlike the integrated circuit industry, where electrical, thermal and mechanical characterisation is undertaken on the complete design, the chips, package and board in SiP solutions are still designed separately.

This approach will not be sufficient to meet the future integration requirements of advanced SiP solutions. The very high level of miniaturisation and extreme reliability required in future SiPs will mean that issues such as thermal and mechanical stress management will need to take into account everything between the point at which heat is generated and the outside of the package. It will be further complicated by integration of special functions into the package, such as sensors, actuator, RF interfaces or power supply components, which may be especially sensitive to heat, stress etc. The application environment in which the SiP will ultimately be used will also need to be taken into account.

To meet these challenges, new architectures will have to be developed. To reach the required level of miniaturization, it will also be necessary to develop advanced assembly and handling technologies for thin wafers and chips. The integration of nano-ICs, sensor chips, actuator components, passives and displays into 3-D architectures will require the development of reliable ultra-thin metallic interconnect technologies.

New low-cost solutions for heat dissipation and thermal and RF shielding will have to be investigated. In addition, improvements in design and simulation methodologies, test strategies and reliability modelling are required. This research work has to be accomplished through the common effort of technology users and technology and equipment providers, as well as the appropriate European research institutes.



Complexity of heterogeneous integration

Design of Heterogeneous Systems

In future electronic systems, the technology boundaries between semiconductor devices, packaging, and system technologies will become indistinct. It will no longer be possible for package design to be done independently of chip and system design. All three aspects will need to be considered simultaneously as part of an overall process. As a result, a broad range of complex design parameters will have to be analysed in order to optimise the complete system, with trade-offs between chip, package and system design. To effectively address higher performance, while at the same time reducing cost across a more diversified technology base, package design is adding to design process complexity, both in terms of design tools and the need for more accurate materials information.

The electrical modelling of interconnects, embedded devices and systems is therefore a very high priority. This will require parameterised models for on-chip/off-chip package co-design for passives and building blocks (for example, frequencies > 3 GHz and high pin-count interfaces). Electro-Magnetic Radiation and Electro-Magnetic Compatibility models for on-chip/off-chip characterization/integration will have to be integrated into

design tools and EDA environments, together with the electrical characterization of interconnects. For on-chip interconnects this will require characterization for frequency spectra in the range 30 GHz to 80 GHz or higher and for off-chip interconnect/packaging, characterization up to 40 GHz, to allow full design synthesis.

The design of SiPs requires cross-disciplinary design capabilities and new methods and tools for chip/package co-design. New design rules and a new design methodology for SiPs and their embedded components will have to be developed.

Design of Reliable Systems

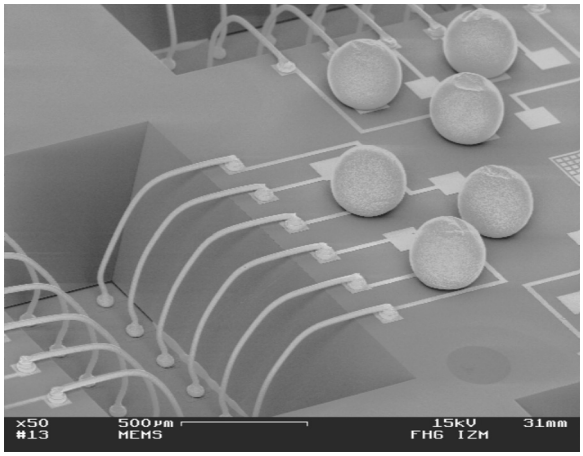
The reliability of future systems will be increasingly important. For example, driver assistance and safety systems will require a reliability similar to that of avionic electronics, but at much lower cost. Product failure rates over the life-span of products will have to decrease from parts per million to parts per billion.

Design for reliability will require developments in the design and simulation phase of product design to provide facilities such as complex thermo-mechanical, thermo-chemo-mechanical and electro-chemical failure mode analysis; the modelling and optimisation of complex interaction-based failure mechanisms; and the modelling of multi-field coupling such as electrical, thermo-fluidic and mechanical coupling. Ageing models for materials and material interfaces (for example, adhesion and interconnect degradation) will also be required to assess life-time performance. Reliability models for life-time estimation will need to be based on nano-material and interface simulation, closing the gap between macro-scale continuum mechanics and molecular modelling. In addition to these design-related models, new field testing methodologies will be needed to accelerate and close the loop between field-testing and design.

Wafer-Level Integration

Following Moore's law, the complexity of future components will increase dramatically. Chips with up to 6000 inputs/outputs are expected, and on-chip and chip-to-board frequencies are likely to double. Even though the energy consumption per transistor will decrease, the total energy demand per chip will increase due to the higher number of transistors and their higher frequency of operation. In addition, future systems will require additional radio-frequency and non-electronic functions such as sensors, actuators, power supply components, passives and displays, which often require the use of alternative materials and special processes. However, integration of these alternative materials and processes into manufacturing often reduces yield and/or increases cost. Ultra high-density wafer-level integration technologies must therefore be able to successfully combine different technologies while also meeting yield and cost requirements.

A number of technologies are being researched to do this. These include using layer deposition techniques to create embedded components, embedding ultra-thin devices into cavities or polymer layers, creating high-surface-area honeycomb structures for integrated capacitors, and nanowires to integrate III/V material (InP, GaAs) and SiGe components. Similarly, new technologies will be needed for the wafer-scale integration of antennas (24 GHz to 80 GHz), photonic compo-



Back-side connections in wafer-level packaging

nents, batteries and energy scavengers, bio-interfaces, micro-fluidics and MEMS. Wafer level encapsulation technologies using nano-filled materials (wafer molding), alternative technologies for 3D-integration (for example, through silicon via technology), new isolation and shielding technologies for RF have to be investigated. To reliably manufacture wafers with such a high degree of wafer-level integration, advanced assembly and handling technologies for thin wafers and chips will need to be developed.

In 3D integration and thin wafer technology the following priorities are envisaged

- Wafer thinning, dicing, handling, thin interconnects
- Integrated shielding (RF and Power separately)
- Chip to wafer integration
- Low temperature wafer bonding technologies
- Technologies for functional polymer layers (chip in thin film layer, interconnection by wafer transfer)
- Functional layer integration (actuators, sensors, antennas, lenses)
- Isolation technologies (RF, micro waves) requiring new substrate technologies
- 3D Integration (vertical chip integration, through silicon vias/ power vias)
- Secure package technologies
- Integration of energy storage and converter
- Optical chip-to-chip interconnects

Substrate-Level Integration

Most of the comments made above for wafer-level integration also apply for substrate-level integration, which represents the next level of interconnect/integration (the substrate on which wafer-level components/systems are mounted). Future board and substrate technologies have to ensure cost-efficient integration of highly complex systems, with a high degree of miniaturization and sufficient flexibility to adapt to different applications.

Priorities

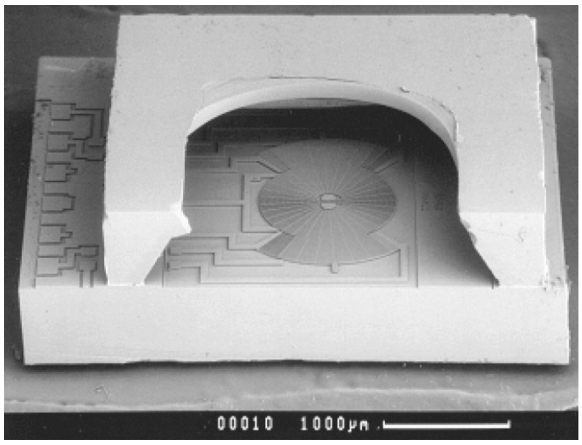
- Embedded devices technologies for MEMS, passives, antennas, ICs, power management
- Lower cost, finer-line and smaller via substrate and interposer
- Impedance controlled wiring
- Flexible substrates (reel to reel manufacturing)
- Integrated optical interconnects/ photonic packaging
- Printable electronics

To reach these priorities new materials for embedding and encapsulation have to be developed such as high-k and low-k dielectrics, high glass temperature polymers and Coefficient of Thermal Expansion matched dies and substrates.

Interconnect, Assembly and Packaging

Due to the higher number of inputs and outputs (I/Os) in complex SoC and SiP solutions, the proportion of the total production cost represented by the package will increase. Cost-effective and reliable technologies with a high manufacturing throughput therefore have to be developed.

Due to the increasing power density in chips there is a requirement for low-cost reliable micro-bumps that can handle high current densities. Chip interconnects will also have to be developed that



Cavity package on MEMS gyro

can withstand high-temperatures (150°C to 200°C or higher), and there will also be a requirement for low-temperature, solderless interconnect technologies and very low cost printable interconnects. Future assembly and packaging technologies will have to support 3D technologies as well as being suited to low-cost high-speed high-precision assembly methods.

Priorities

- Package stacking (reflow soldering of stacks)
- Mechatronic packaging (special mold compounds, lead frame technologies)
- High pincount power packages
- Integrated capping/ shielding technologies
- High precision assembly of optical components (self alignment/ alignment support)
- Die stacking (higher alignment accuracy, thin die (10µm) handling)
- Low cost advanced cooling concepts and materials
- Technologies for miniaturizing package profiles (3D packaging)
- Low temperature packaging

Testing and Quality Management

Due to the higher value of a system compared to a single component, quality management is taking on even more significance. Test procedures and requirements must be considered during the design phase and integrated into the production flow. Not only do more functionalities have to be tested in a system compared to a component, these functionalities are increasingly complex. Accelerated reliability testing is also needed to fulfil customer requirements in a reasonable amount of time and at an appropriate cost.

Priorities

- Solutions to the 'known-good-die' problem
- Low cost wafer-level or die-level system test and burn-in
- RF and high-speed mixed signal wafer level test
- Solutions for integrated sensors, MEMS, fluidics
- Low cost probes/contactors for massive parallel testing
- Fully integrated test data diagnosis flows to handle SiP
- Fault models to handle assembly defects by electrical test
- Adaptive test flows to handle statistical process/device parameter fluctuation
- Automated test pattern generation

Applications for Nanotechnology

In the midterm (> 2010) nanotechnologies will be used to improve material properties, to improve device functionality and to create new interconnection technologies.

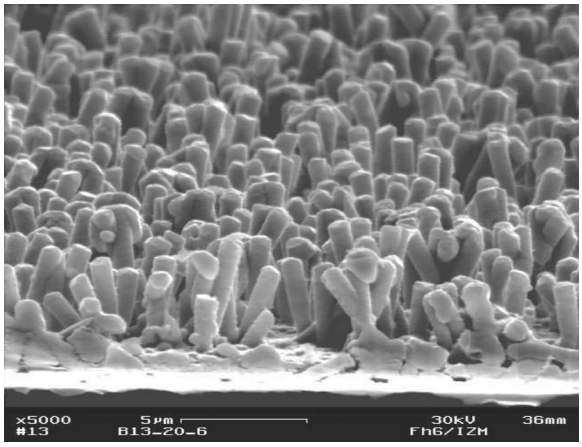
In the area of improved materials it will be possible to adjust parameters such as electrical resistance, thermal conductivity and coefficient of temperature expansion (for example, in moulding compounds) by the addition of nanoparticles. True nano-structured materials will provide new solutions for high-k dielectric capacitors and low-k dielectric inductors, improving the quality factor of these components. They will also provide improved thermal performance. In the area of interconnect and assembly technology, nanostructures will allowing surface activated bonding and provide nano-pillar contact bumps.

In the longer term (> 2015) nanotechnologies will be used for further improving interconnection and assembly technologies. Possible applications include carbon nano-tubes for heat dissipation and interconnects, low temperature interconnects using nano-structured surfaces and self positioning/assembly of die/devices and molecular bonding. It will also be possible to model nano-particle filled materials at the molecular level to improve their performance.

Generic Topics

Heterogeneous Integration concepts must provide technologies at lower cost together with comprehensive risk assessment, shorter time-to-market

cycles and a higher degree of flexibility. A modular technology approach will be needed to achive these objectives. Zero-defect technologies (both at package, chip and integrated system level) should help companies to create right-first-time designs.



Nanolawn

In addition, future Heterogeneous Integration concepts must take environmental issues into account. Chemicals and materials should have minimum impact on the environment and people. New concepts will also be needed for the repair and re-use of modules.

Priorities

- Environmental issues
- Lead-free electronics
- Halogen-free processes
- Reduced energy consumption processes
- Non-destructive disassembly/rework of SiPs
- Concepts for long-term availability of SiPs
- Technology modularization
- SiP tool box (materials, equipment, technologies, interfaces, test)
- Short time-to-market processes
- Zero-defect technologies (for both package and influence on chip)
- Cost reduction and reliability improvement

Domain 'Equipment and Materials'

The Materials and Equipment roadmap of ENIAC will be based on the ITRS roadmap, highlighting specific European strengths in the domain and augmented with additional requirements from the other technology domains, specifically More than Moore, Heterogeneous Integration and Beyond CMOS.

Substrate materials

Bulk silicon substrates are still considered to be viable for introduction of the next diameter generation beyond 300-mm wafers. However, past experience has shown that such introductions are very costly in terms of time, resources and investment, especially for material suppliers. While the industry seems to agree that the next diameter will be 450mm, there is no consensus yet on when introduction of 450-mm wafers needs to take place. This, however, is a key decision, because around eight years of development time is needed between preliminary research and volume production on a new wafer size. If, for example, 450-mm wafers are required in 2012, wafer makers must start work now!

Other challenges related to bulk silicon substrates are less well described but nevertheless critical. Constant improvements need to be done at the substrate level to accompany the constant shrinkage of device dimensions. Of particular interest is the development of defect-free crystal ingots/wafers, the improvement of flatness/nanotopography, and the systematic reduction of particle size and density as well as residual impurity levels on back /front side.

Volume production of thin Silicon-on-Insulator (SOI) already addresses partially depleted MOSFET architectures. The Si thickness ranges according to design rules and applications between 100nm and 35nm. For fully depleted device architectures the layer thicknesses targeted lie between 15nm and 30nm. The present develop-

ment of thin SOI focuses on thinner top Si layers, on improving the surface roughness to minimize local thickness variations for sub-65nm devices, on tighter layer thickness control, and on wafer edge roll-off to further reduce the impact of SOI edge exclusion.

450-mm silicon monocrystal

The strength of the layer transfer technique is that it makes it possible to create a fully engineered substrate, tailored to the requirements of an application by properly choosing the active layer, the buried dielectric and the base substrate. Three fields are highlighted: enhanced mobility, improved thermal conductivity and high impedance substrates.

Starting from an SOI wafer there is an evolution from Si (100) as the active layer towards Si (110), strained Si, and even Ge to provide mobility enhancing substrates. The mainstream choice for the buried dielectric is thermal oxide but work is ongoing to evaluate the use of alternative dielectrics or buried multi-layers for improved thermal conductivity and reduction of hot spots in the top IC layer. Furthermore, deposited dielectrics open the possibility of including buried patterns in the dielectric layer. Lastly, the substrate offers several options such as high resistivity Si for RF applications, or being non-silicon.

Because it exhibits much higher mobility than Si, both for electrons and for holes, pure Germanium is considered as a longer term solution to address sub-32nm nodes. Ge offers better integration compatibility with high-k dielectrics and with GaAs epitaxy, which could be an enabler for optical interconnects.

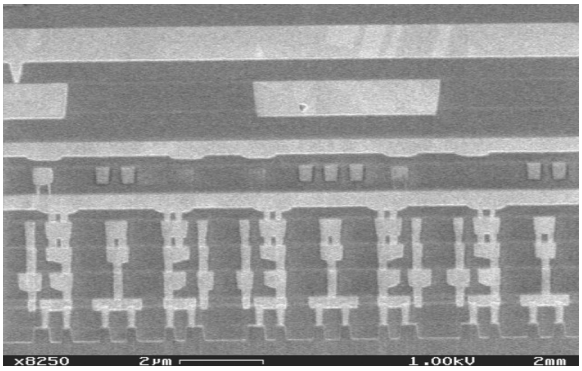
In conclusion, more added value will come from engineered substrates to help device developers overcome the hurdles imposed by Moore's Law.

Processs- equipment and chemicals

Historically, (poly)-silicon, silicon dioxide, silicon nitride and aluminum based materials have been the materials of choice for semiconductor devices. In the last decade, however, it has proven impossible to further extend dimensional scaling with this set of materials alone. A multitude of new high-performance materials with engineered electrical, mechanical and chemical properties must be introduced to expand Moore's law and allow fabrication of scaled devices that operate at higher speed and/or lower power. A huge material science effort is required to deliver the necessary properties, involving the selection, demonstration and integration of appropriate chemistries. For materials processing, established processes such as Chemical Vapor Deposition and Physical Vapor Deposition are now being complemented with processes such as Atomic Layer Deposition, electro-plating, and selective deposition processes of silicon and other materials. New etching chemistries also need to be developed for the many new elements introduced into semiconductor manufacturing.

The introduction rate of these new processes and materials has increased dramatically. With the end of classical CMOS scaling in sight and the emergence of post-CMOS logic and memory devices between 2013 to 2016, further acceleration in the rate of

new material /process introductions is needed to allow the industry to follow Moore's Law.



Multilayer interconnect CMOS structure (9LM, 90-nm)

The parallel development of heterogeneous devices is also fuelling the demand for new high-performance materials and processes. Not only is the computing power and memory capacity of devices increasing, the functionality of these devices is increasing rapidly as well. Wireless RF interfaces, embedded memories, micro-electro-mechanical systems (MEMS) have already been introduced, either as System-on-Chip (SoC) or System-in-Package (SiP) solutions. Embedding even more diverse functionality, such as optical interfaces, chemical and bio-chemical sensors, micro-fluidics, power generation and storage, is foreseen.

Finally, new computing technologies currently being researched, such as molecular, quantum and DNA computing, rely on the nano-materials elaboration and processing control of mostly unexplored chemistries.

Requirements on the processing technologies to generate these new devices will be increasingly demanding, in 'More Moore' as much as in 'More than Moore' and Heterogeneous Integration, and even more demanding in 'Beyond CMOS'. These requirements can be outlined for the extension of CMOS technology along the following five guidelines.

Lower processing thermal budget
The increasing number of process steps and the shorter diffusion lengths in devices imply ever lower processing temperatures. Novel (metal-organic) precursors and improved equipment to introduce them in the reaction environment have to be developed. Also non-thermal activation by, for example, photons or radicals will increasingly be deployed in processes. Not only the deposition process itself, but also the etching and surface preparation steps or post deposition treatment steps will have to comply with the lower temperature requirement. This calls for novel cleaning and treatment technologies, deploying novel chemistries and/or non-thermal activation with photons or radicals.

Higher aspect ratio step coverage
Further CMOS scaling and post-classical CMOS fabrication of 3D devices will demand deposition/etch technologies that have more demanding step-coverage control, or technologies that result in improved planarity. For some applications conformal deposition is required, while for others directional deposition is required. Further development of technology platforms and chemistries for conformal deposition and removal is required. Catalytic, super-conformal technologies in dry or wet environments, and selective deposition technologies will have to be developed to preferentially fill narrow structures.

Film Interface Control
Layers of atomic thickness of different materials will be used, which means that cleanliness and precise atomic-level control of interfaces will become very important. New and improved cleaning and priming technologies, in-situ interfacial measurement and control techniques, and improved control of the wafer environment must be developed for all process technologies.

Novel Material Properties
The range of accessible material properties of thin films, both for mainstream and special appli-

cations will have to be expanded. New technology platforms to deposit multiphase materials such as controlled nano-porosity materials and nano-laminates, bio-materials and self-assembly layers must be developed.

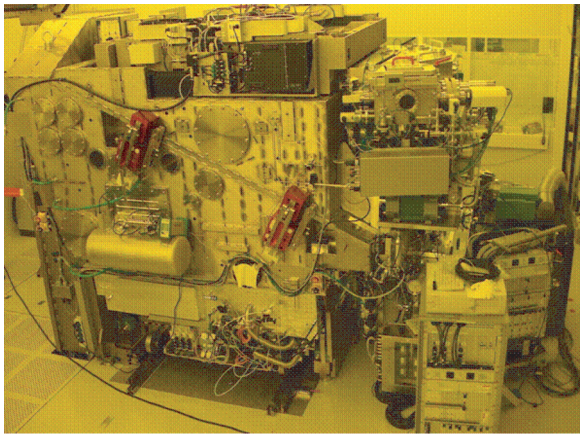
Flexible Technology Platforms

Rapid introduction of new materials in the device development and manufacturing environment for products with potentially short lifecycles is only possible in an economic way if the employed deposition platforms are flexible. Flexible deposition platforms allow rapid development of new materials to pilot line maturity. Increased deployment of a wide variety of new chemicals calls for improved Environmental Safety and Health procedures to allow for the timely development of abatement and recycling technologies, shipping and handling procedures, so that new chemicals can be deployed quickly without any adverse impact to the environment.

New devices and computational principles emerging from research rely basically on barely explored supramolecular chemistries. Elucidation of the functional principles, demonstration of the molecular fabrication feasibilities and development of the considered computation algorithms and their realization opens up opportunities for huge chemical, device and principles research.

Lithography

The capability to shrink devices has been the business model of choice for the semiconductor industry, simultaneously improving performance in several areas while also reducing manufacturing costs. It is foreseen that this trend will continue over the coming decades. Optical lithography has been the engine for this model and in the near future will be extended to Extreme Ultra-Violet Lithography, the last optical technology currently foreseen. To keep this mass fabrication engine going, several requirements need to be met. Firstly, making use of a reducing replication technique, which has the capability of high throughput and which can simultaneously meet overlay requirements on previous layers. High Numerical Aperture immersion technology with fluids of high refractive index addressing the 45 nm and 32 nm node will be pursued. EUV litography should then be pursued to the limit of its capabilities, now estimated to be at the 13-nm or 8-nm node.



Extreme ultraviolet lithography research tool

Besides this there are opportunities to develop maskless printing techniques and imprinting technologies. Maskless printing technologies are particularly important for Europe, because a large part of the European Semiconductor industry is geared to producing application specific semiconductors. Maskless lithography (ML2) will facilitate this by offering good time-to-market for new designs and low cost manufacturing technology for small series.

Imprinting technologies get considerable attention since it represents the smallest replication technology currently known. Problems to be resolved include overlay capability, throughput, stamp life, stamp mastering and inhomogeneity in the polymer residue thickness.

Special equipment in the 'More than Moore' and 'Heterogeneous Integration' domains will be needed for printing on glass or flexible substrates for human interface applications.

Masks

Lithography may be key for miniaturization, but it involves very expensive tools and masks. In particular, the zero defect requirement for masks is making them very expensive. Therefore it is critical that a large amount of R&D effort is put into exposure equipment, resist materials and resist processing equipment; mask making and mask making equipment and materials; and metrology equipment for critical dimension measurement, overlay control and defect inspection.

We envisage a roadmap that will split by 2010 into companies that implement EUV for the most critical layers in order to meet the technological challenges and companies that push the limits of current optical lithography using expensive reticle enhancement technologies and new material solutions. Mask blank suppliers need to do research into both avenues and support both communities with new and improved blank materials. However, extensions to optical lithography will probably reach their limit at the 22 nm node if not before, which will impose implementation of EUV on the whole industry.

This will shift the focus from defect-free masks to defect free mask-blanks, since multi-layer defects will be difficult to repair, if not irreparable. Additionally the uniformity requirements for future nodes require sophisticated deposition tools, which combine low defectivity with very challenging uniformities.

Mitigating defects either by in-situ repair or by actively preventing defect generation and defect migration will probably not be enough. In-situ and ex-situ measurement techniques will be required to differentiate between defects that print, defects that do not print and false defects that result from measurement but have no influence on the blank performance. Particle surface interactions will play a key role and need to be investigated together with cleaning and repair methods. EUV has clearly the advantage over other techniques in having a simpler mask type than that needed for reticle enhancement in optical lithography. Beyond the 22-nm node, however, similar reticle techniques will probably be needed for EUV as well. In particular, investigations need to be carried out to explore a process window that comprises the whole process from blank to wafer.

Mask writing

With the introduction of Optical Proximity Correction and Resolution Enhancement Technology, shaped beam e-beam tools have become the state-of-the-art mask writing tool. However, reducing the minimum pattern line-width has an adverse impact on the throughput, which has always been a limitation of e-beam equipment. Throughput is never high enough to satisfy the customer. E-beam development programs must therefore focus on throughput.

In addition, resist processes and metrology are instrumental to the successful use of e-beam lithography and the requirements for these also become more stringent as line-width is reduced. This will be another important consideration for e-beam development programs. It is probable that only massively parallel e-beam systems delivering the highest resolution in each beam will be able to solve the challenges for technology nodes smaller than 45nm.

The mask writing process will and can benefit from the currently started European initiative to develop Maskless Lithography for 45nm and beyond.

Mask inspection, metrology, and repair

The goal of photomask quality control should be to detect defect growth at a point where any defects are just beginning to form but are not yet yield-limiting. A carefully developed mask requalification inspection strategy should be implemented to optimize mean time to detect of any defect growth resulting from prolonged reticule use.

However, a major problem for the industry is real-time line-width measurement below 10nm. Of the various techniques currently available, Scanning Proximity Probes are the most appropriate in terms of accuracy and ease of measurement. However, the technique needs to be urgently enhanced to enable high-speed imaging. The ability to perform high-speed in-line metrology at these dimensions will put the European semiconductor industry in a world-leading position.

Further developments in mask repair are necessary to avoid charging effects and to improve the throughput and metrology limitations.

Metrology

R&D into process technologies for sub-32 nm nodes requires advanced measurement capabilities that do not at present exist. Action lines where breakthrough improvements for future technology nodes are required include:

- Quantitative Impurity/Dopant profiling with sub-nm spatial and depth resolution: the introduction of very thin layers and 3D-structures puts stringent requirements on profiling resolution, 3D-capabilities and very localized analysis.
- Carrier/resistivity profiling: the introduction of advanced implants and anneal processes has led to significant differences between dopant profiles and active carrier levels, which imposes new requirements for probing active carrier levels.
- Compositional analysis: many thin layers require new methods to probe their composition with high quantification accuracy, sub-nm depth resolution analysing the dominant influence of interfacial composition, and high spatial resolution (nm). Also information on the chemical bond structure is required.
- Structural analysis: novel device structure concepts, such as strain in transistor channels, side walls, CNT-contacts, require probing the crystalline nature of very thin films or crystalline properties with very high spatial resolution.

Domain 'Design Automation'

A central theme in managing the complexity and manufacturability of nanoelectronic systems is the increasing reliance on Electronic Design Automation (EDA). EDA is the essential link between application requirements derived from societal needs and their implementation as SoC or SiP in the 'More Moore' and 'More than Moore' domains. This link must be formal (to capture the needs and drive the implementation) and able to handle the required complexity, taking into account heterogeneous concepts such as abstract processes descriptions, verification, physical implementation, manufacturability etc.

Such EDA systems must be capable of capturing formal design specifications written by System Houses, of allowing high-level system and architecture exploration within the underlying constraints of available implementation technologies. All aspects of product development, including digital, analog/mixed signal, power electronics, and embedded software in conjunction with non-electrical components like MEMS must be embraced. This will demand expertise drawn from the many different disciplines involved in product design (specification definition, HW and SW co-design, circuit design, verification and validation, and physical implementation with constraints for test and manufacturability) to be built into EDA tools.

The proportion of software development and architecture exploration tasks in the overall design flow of a complex SoC or SiP is growing rapidly when moving to more advanced technolgy generations. A major component of that growth is the increasing focus on Design for Manufacturability – a new constraint that builds the feasibility of physical nanoelectronic implementation into the design process. This is a completely new world for the designer that impacts the fundamental economics of manufacturing the device, allowing non-zero yield from the outset, rapid yield improvement during product ramp up to gain market share, and maximum yield in large volume manufacturing.

A consequence of the increasing number of design tasks that have to be performed and their complexity is already leading to a phenomenon known as the design gap – the difference between what can theoretically be integrated into systems and what can practically be designed into them. Advances in EDA tools that automate many of the necessary procedures are the only way to close this gap.

ARTEMIS and ENIAC complementarity

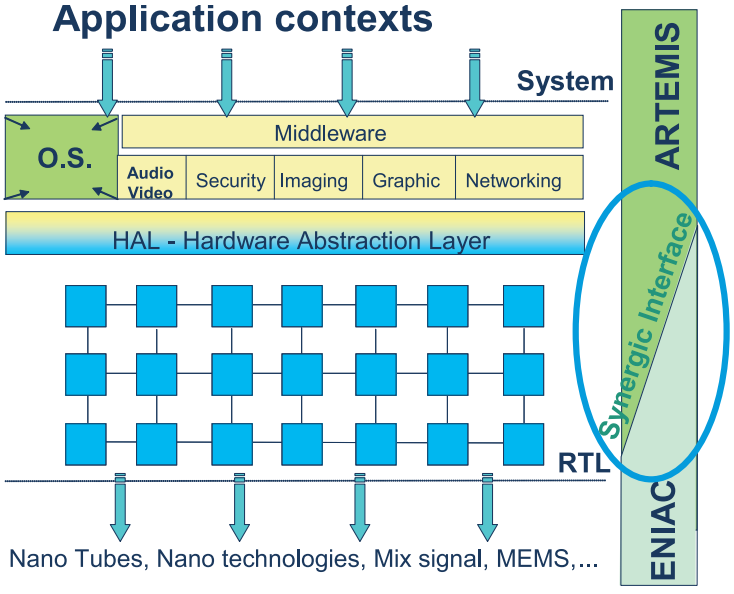
ARTEMIS, the sister organization to ENIAC, will focus research into EDA tooling that supports the system-level approach – namely tools that are designed to facilitate formal specification and architectural exploration using new techniques for the efficient design of next-generation embedded systems. These tools will address both hardware and software as well as the need to reliably predict system behaviour in real-world environments. They will typically follow a top-down route, from system specification down to a silicon layout description.

ENIAC will mostly handle the tasks related to hardware implementation with a specific emphasis on designing for low-cost manufacturing and high added value (a maximum number of good chips on the wafer). However, this will only be feasible if behavioural descriptions for the implementation technologies can call upon accurate models of the underlying physical materials and processes. The same is true for the non-electronic behavioural models required to assess thermal and mechanical behaviour, and the models needed for new types of device resulting from research into MEMS and NEMS solutions for sensors and actuators. All this falls within the ENIAC charter, but is also essential for execution and implementation of the ARTEMIS Strategic Research Agenda.

There is no hard wall between the levels of abstraction dealt with by ENIAC and those dealt with by ARTEMIS. Indeed, without cooperation with ARTEMIS regarding the methods and models used at higher levels of abstraction, the usability of the lower-level models generated by ENIAC directed activities cannot be guaranteed to be either useful or reliable. Joint studies into design methods for architecture exploration are therefore conceivable, facilitating the interface between system designers and hardware/software IP developers through the use of formal executable specifications. Application-specific platforms for hardware and software can be used as full application demonstrators, defined by ARTEMIS but with joint realization through ENIAC's hardware implementation solutions.

In the field of embedded software, ARTEMIS will address the specific problems of application software, including the operating system and hardware dependent software drivers. ENIAC will focus mostly on software that is intimately related to the hardware blocks in which it is embedded (subsequently referred to as 'firmware'). The hardware abstraction layer will form a common interface between the two. ARTEMIS will own validation and verification of both functional and non-functional system properties, relying on ENIAC support for models. Additionally, advances in state-of-the-art Design for Manufacturability and Design for Uncertainty (statistical design) or Design for Dependability (fail safe systems) will bring with them the need for intimate links across all levels of the design hierarchy for practical implementation.

A methodology to handle these tasks could be the one proposed in the 2005 MEDEA+ EDA Roadmap. This separates front-end and back-end thanks to a Model Driven Design for the abstract levels plus implementation through a Network-on-Chip together with customised IPs that are designed for manufacturability. This would lead to an application design platform, encompassing formal systems specifications, embedded software layer design, network-on-chip, and IP-reuse-based implementation / verification / DfM, where both ARTEMIS and ENIAC could more easily manage their contributions in a continuous design flow, and where architecture and implementation constraints coming from front-end decisions could be more efficiently handled.



ENIAC and ARTEMIS have a synergetic interface

In the full design flow, there is a need to link within the same environment both design specifications and technologies for manufacturability. This can be achieved through Predictive Technology CAD linking technology process steps in equipment to device feasibility and characteristics in the manufacturing plant, the results being used to cope with circuit performance and manufacturability. Such a complete flow allows the equipment, process, device characteristic and manufacturability domains to be linked by simulation and optimised globally.

Priorities

Heterogeneous systems

The ability to cope with the design of heterogeneous systems is one of the key priorities identified for Design Automation research in the coming years. Because the scope of ENIAC goes as far as the year 2020, it is not possible to give an exact definition of what a heterogeneous system will be, given that such systems will evolve and change over time. However, one characteristic of these heterogeneous systems will almost certainly be the presence of analog, mixed signal, RF and digital processing within the same System-on-Chip (SoC) or System-in-Package (SiP). Passive component integration and the integration of devices such as MEMS, sensors, small display devices, etc. will be commonplace, either integrated onto silicon or assembled alongside silicon-based technology. These assemblies will increasingly be interconnected three-dimensionally, and controlled by an ever- increasing amount of software.

The challenges in Design Automation in heterogeneous systems are manifold. First of all, designs need to start from formal specifications, and they need to be moved to higher levels of abstraction (from TLM today to formal executable specifications), including the development of the corresponding synthesis solutions. IP libraries specific to the identified Nanoelectronics application domains must be developed that are compatible with the higher abstraction level design flow and customized and designed for manufacturability. Low-power by design implementations must be introduced, as well as design for signal integrity at chip, package and board levels, and finally, design for manufacturability constraints at every step in the design process need to be handled and implemented.

Design for Manufacturing

Design for Manufacturing will bring major new innovations in areas such as post processing, for example, re-shaping and re-configuring chip layouts after GDSII taking into account performance constraints that come from design and low-cost constraints that come from manufacturing. This step is far from being achieved today because for the first time it will involve the simultaneous dynamic handling of information originating from both the front end and back end.

Realizing these expanded design-flows will not only require additional views of the cell library but also basic research to efficiently model much more sophisticated nanoelectronic technologies. Additionally, transformation of variances in the basic physical parameters into those of more abstract library models (statistical simulation) and limiting the amount of silicon production/testing required to verify this is another major challenge.

Yield optimisation by simulation of the design-space will be another area for investigation. In future, estimation of the effect of systematic yield hazards on the final yield of a very complex SoC will become extremely difficult. Given the very large expected increase in non-recurring expenses and development costs, this will have to be done at an early stage of the design cycle and will be an indispensable step. Given the number and complexity of future design rules, the fact that they may not be orthogonal and the variance in fabrication tolerances, this target can only be achieved by means of very complex simulations. There may even be different cost functions that need to be applied to a SoC/SiP depending on the specific application domain.

Yield-aware design flows from ESL level down to placement and routing are another essential long-term objective because they will drive the market competitiveness of the final product. However, bearing in mind the timelines and the complexity, this most challenging of problems may be something of a moving target.

Effective reuse of optimised hardware IP blocks will require a major standardisation effort as well as the reshaping of entire IP libraries to make them manufacturability-aware and customized to specific application domains.

Design for Reliability

Design for Reliability concerns the design of dependable systems for safety critical applications that have some level of reconfigurability to compensate manufacturing defects or defect that occur in the field.

Achieving Design for Reliability will require a range of research activities including gaining a basic understanding of degradation mechanisms, a thorough study of relevant degradation mechanisms by stress experiments and failure analysis, and the generation of lifetime extrapolation models and associated design rules. Extended library and routing optimisations will need to be developed to meet reliability constraints through identification of problematic sites (e.g. electromigration for vias and connections: critical geometry dimensions and current densities in vias). This will lead to automatic mitigation of critical sites according to generic and technology-specific rules during the design process (eg. by setting of double vias as an example).

In addition to performance and yield, Design Verification Methodologies will need to be adopted for reliability. This will require the development of tools for layout analysis of reliability-related electrically critical structures, for a reliability-aware design flows, for improved place and route, and eventually for reliability simulation.

With higher transient currents, a shrinking distance between components, and a significant decrease in the signal strength on nodes (at the level of one femtocoulomb), signal integrity problems may be a significant road-block if they are not properly addressed both at chip and package levels. In particular, the signal strength on nodes will be low enough that natural background radiation interacting with device materials (causing Single Event Upsets) could cause SoCs or SiPs to malfunction. Appropriate process and design solutions will have to be put in place to minimise these 'soft defects'.

Cooperation with SMEs

New EDA solutions developed in European programs need to be put on the market as soon as possible so that they are available to users. In the past, however, Europe has been slow in this respect. In future, serious consideration should be given to encouraging cooperation between specialist SMEs and large European companies to create a critical mass that will move the European EDA business forward. The high level of EDA expertise in European universities and start-ups is a good starting point from which to launch such initiatives and could contribute to keeping strategic advantage and employment in Europe.

Research infrastructures

Europe has a world-class R&D infrastructure for advanced CMOS process technology development. This not only includes the required knowledge base, provided by European centres of excellence and their links with academia. It also includes extensive joint-venture investment in the state-of-the-art wafer fabs needed to develop and industrialize new CMOS processes. The success of this multi-dimensional R&D infrastructure in keeping Europe at the leading edge of the ITRS roadmap for semiconductors is an excellent example of academia/industry collaboration.

In order to maintain Europe's world-class position in 'More Moore' research, this R&D infrastructure will continue to need new investment in both capital equipment and human resources. As CMOS feature sizes reach 45 nm and beyond, the need for new lithography techniques for scaling feature sizes and novel transistor structures for improving device performances will make research programmes in Equipment and Materials some of the most pressing.

In the areas of 'More than Moore' and Heterogeneous Integration the required competencies are far more diverse than for CMOS. They are, however, less dependent on large capital investment. In these areas the challenge will be to create research networks that will bring together expert knowledge in many different yet equally critical competencies. Much of this expert knowledge already exists at various locations across Europe, but the absence of a 'cohesion factor', such as the need to access state-of-the-art wafer fabrication facilities, has left it somewhat scattered. In the same way that European investment in state-of-the-art wafer fabs became a catalyst for cooperation in 'More Moore' research, a catalyst will be needed to unite the players in 'More than Moore' and Heterogeneous Integration. That uniting factor must be the realization that Europe's success in nanoelectronics will depend on an accelerated transfer of multi-disciplinary academic knowledge into socially relevant products and services, and the acceptance of the fact that much of that knowledge is located in a multitude of companies dispersed across Europe.

European 300-mm R&D ecosystems

The Strategic Research Agenda for Nano-electronics in Europe therefore needs to be driven by a core group of industrial players and academic institutions that can recognize the challenges involved and pull together the necessary resources. In doing so, it will be able to use many of the best-practice methods already learned from Europe's highly successful 'More Moore' collaborations. However, the research programs that stem from this agenda will reach much further than those in 'More Moore' research, because many of the competencies needed in nanoelectronics, especially in the areas of 'More than Moore' and Heterogeneous Integration, lie within the wealth of SMEs at the heart of Europe's economy.

Because many of the devices that will result from research into 'More than Moore' and Heterogeneous Integration will be based on silicon wafer processing, Europe's existing semiconductor research ecosystem can act as a hub for knowledge sharing as well as providing shared facilities such as clean rooms and prototyping equipment.

Next to the mandatory improvements to close the design gap in 'More Moore', the areas of 'More than Moore' and Heterogeneous Integration will also open up unique opportunities for Europe's EDA industry as design flows and tools that were originally developed for digital design will need to be redefined and extended to cope with the many different technologies that will go into future nanoelectronic devices. It is not capital investment that is required in this domain but rather investment in creative people and methods of making them more productive.

The 'Beyond CMOS' domain will push the boundaries of scaling to the point where radically new transistor structures or computing architectures will need to be developed. Current research candidates include devices such as carbon nanotube transistors and molecular memories, and it is likely that new 'bottom-up' approaches to device fabrication will have to be combined with traditional 'top-down' technologies into a single nanoelectronics manufacturing process. In this domain, the selection and filtering of ideas is a challenge in itself, requiring a great deal of parallel evaluation and structured communication. While the short-term impact may be low, this research must be supported today in order to prepare the information processing technologies that will take over from CMOS based technologies in a 10 to 15 years time frame.

While the role of European academia will be crucial in realizing the Strategic Research Agenda, this academia increasingly experiences difficulties in gaining access to state-of-the-art research infrastructures for nanoelectronics. The budgets available for investments and operations in the individual laboratories do not match the pressing needs of advanced materials and device research and device implementation, and the gap widens whenever a new technology is introduced.

PRINS project

In order to provide a coordinated solution to this challenge, a public-private partnership called 'Pan-European Research Infrastructure for Nano-Structures' (PRINS) is envisaged. A proposal addressing the PRINS project was submitted to ESFRI and accepted in its shortlist of candidates for (partial) funding by the EC in the period 2007-2013 under the 'Capacities' heading in the 7th Framework Programme.

The PRINS project aims at constructing a research infrastructure (especially advanced equipment and facilities) to enable European research into the ultimate scaling of electronic components and circuits. The infrastructure will be interdisciplinary by allowing the convergence of top-down technology, which is today the main enabler of Moore's Law, with bottom-up methods derived from fundamental disciplines such as materials physics, chemistry and nanobiotechnology.

To maximize the cost-effectiveness and efficiency of implementation, the PRINS infrastructure will be distributed over a limited number of existing sites, grouped around IMEC, CEA-LETI and Fraunhofer VME as major hubs, with a specific technical focus for each site. The capability of fabricating disruptive nanometer-sized functional structures needs to be fully addressed at the European level by leveraging the complementarity of the tools and by implementing an easy exchange of wafers between the selected sites of the research infrastructure. The three research institutes will act as the main integration centres for ultimate silicon processing and heterogeneous integration, while the many linked academic centres will be able to make optimal use of the PRINS infrastructure. The network of R&D centres will be strengthened and supported by the contributions from SMEs and other industrial partners.

The PRINS research infrastructure will contribute to realizing the goals of the ENIAC Strategic Research Agenda as it will enable research on the ultimate silicon applications, on emerging information processing devices, as well the exploration of the novel opportunities created by top-down/bottom-up convergence.

Science and education

A Scientific Community Council has been installed as the highest body representing the scientific community in ENIAC. It will consist of national delegates representing the academic community for each of the respective countries in the European Union and of the Associated Countries together with topical academic experts seconded to the various ENIAC Working Groups and to each of the Domain Teams working within the Working Group for the Strategic Research Agenda.

The Working Group Science and Education will be the forum where representatives of academia (the 'supply side') and of industry (the 'demand side') meet and address two major areas of interest to the scientific community. This Working Group will enable efficient communication between industry and academia, provide a strategic outlook with respect to the SRA and coordinate important aspects of its execution, and coordinate all Education & Training aspects of relevance to ENIAC.

It is the mission of the nanoelectronics-related research teams in academia to perform groundbreaking research in areas such as materials and process steps for electronic devices, interconnect and packaging technologies and the design, fabrication, characterization and application of nanostructures and nanosystems; and to provide education and experience for graduating students to allow them to successfully pursue a career in nanoelectronics.

By matching the 'technology push' from the science and engineering community with the 'market pull' of large industrial partners and end-users, the Strategic Research Agenda will ensure that the research coordinated under it is industrially and economically relevant and maximally beneficial to society.

This undertaking will indeed engage academia and industry alike, bringing together the leading-edge research of the science and engineering community (carried out at universities and research organizations), the specialist know-how of SMEs and the industrial muscle of large companies to create the leverage and critical mass necessary to obtain breakthrough results.

Education and training needs

The semiconductor industry faces huge technical challenges as it pursues the development of systems based on nanoelectronics. In this pursuit, the availability of skilled Human Resources is of vital importance. In the digital age, 'brain power' is a competitive advantage for individuals as well as for companies. Consequently, the European semiconductor industry must adapt and develop its 'Human Capital' asset, expanding and strengthening Europe's nanoelectronics industry talent pool.

The knowledge-intensive nature of the nano-electronics sector requires a global approach harnessing resources from the private, public and academic sectors. The semiconductor industry must forge closer cooperation with the public and academic sector with the aim of defining the skills needed for the new information-intensive economy and in those areas where the modes of collaboration have been identified, of setting up a common Education and Training Framework. Design, manufacturing, and R&D management are the three domains that have been identified as the pillars of a collaborative initiative in Education and Training.

VLSI design work for today's high performance circuits faces a drastic paradigm shift, as it moves rapidly towards fully integrated solutions, embedding Intellectual hardware and software functions

in one SoC or SiP. Silicon systems designers must master a whole range of critical skills and capabilities but possibly more importantly they must be able to work in teams. Indeed, silicon design work will increasingly require excellent interactive communication skills on top of basic technical know-how. A particularly demanding development in the skill-set required by designers is the combination of both hardware and software talents. Moreover, in order to master nanoelectronics systems, engineers and scientists will increasingly have to rely on interdisciplinary competencies related to electronics, mechanics and materials sciences, as they deal with thermal and transport aspects, as well as quantum phenomena. Interdisciplinary skills are also needed in order to combine technological performances, business constraints, and societal aspects, including market changes, cost and return-on-investment considerations, legal and patent issues, and human interfacing. Thus it is concluded that interdisciplinary approaches are critical in order to make a highly complex and innovative activity such as SoC design more adapted to the present-day needs.

Modern semiconductor manufacturing is characterised by high complexity but also by key requirements such as development speed (lowest possible time to volume), optimised cost structures, and highest quality (zero defects). In order to meet these requirements, the European semiconductor industry needs experts who are trained to work with extremely complex tools, using advanced logistics and scheduling systems, and who have also mastered the most recent nanoelectronic manufacturing processes. Therefore, each company needs intensive education and training at the tool level, involving automation and transport systems, planning and logistics, and advanced process control systems. Additionally, skills in maintenance are required in order to optimise the use of very capital-intensive new manufacturing facilities. As most of these skills concern methodology rather than company-specific aspects, there is a wide opportunity for co-operation and for exchange of instructional material, teachers and students between companies.

These new challenges in design and manufacturing require new forms of communication and collaboration, in particular the ability to create and maintain trust and productivity in organizations that are rapidly changing. In order to face the changing environment, new managerial skills are required leading to a global mindset and the ability to deal with the complexity of a problem and to understand the various parameters involved. None of these objectives can be reached without creating a sufficient level of team spirit and motivation within multidisciplinary teams, very often working in various locations around the globe in different time zones. New R&D management principles must be developed and shared, involving advanced communication methods and tools (such as distance learning, web-based information sharing), intercultural aspects, and information searching and sharing techniques.

How can one ensure that such a framework can be successfully set up, meeting the objectives discussed above regarding content, communication channels, tools and information sharing? The answer boils down to the selection of relevant Education and Training providers, to the setting up of a suitable process for defining and prioritising the needs from a demand perspective. This will allow the development of an action plan and an Education and Training roadmap that will ensure the effective management of efficient and flexible Education and Training programs.

Selecting providers

First of all, it is important and fair to state that there are many players today in Europe who are actively involved in providing high-level support, education or training in one or more of the domains discussed in this document. A lot of expertise is indeed available in Europe in universities, research centres, commercial training

providers and industry, but it is typically somewhat dispersed and often not in an adequate format or with the right emphasis.

Universities are obviously first in line for providing basic education in a generic fashion. Today new programs are being set up at universities to cope with the new demands, the requested skills and the needs of industry, research and society. This is to a large extent driven by the urgent need for a stronger interdisciplinary approach. Most universities in Europe are at this very moment refining and reshaping their curricula to target more uniform Bachelor / Master programs. Universities also continue to strive towards providing unique educational offerings that differentiate them from their competition in order to attract students from all over Europe. This reshaping and redefinition of the curricula and the format of education, together with the stimulation of educational choices and programs, is indispensable if Europe is to respond to the growing need for skilled engineers and researchers. It also offers a unique opportunity for educational opportunities and requirements to be triggered and supported from the demand side.

In addition to universities, some research centres and commercial training providers have built up specific educational programs, training approaches and formats over the years in order to complement offerings from academia. Many provide a stronger emphasis on industrial and production-related aspects and on the use of new technological training tools. These centres can often offer customized programs in a flexible way with a much faster response to the needs of their industrial customers. It will be very important to select and bring together suitable players with complementary goals, visions, programs and approaches, who are willing to respond to the needs in a constructive way.

Setting the strategy

The requirements regarding content and training methodologies will have to be captured in a systematic way and should result in a strategic Education and Training plan. This can be done in a three-step approach.

The first step is the collection of input from the demand side on specific educational requirements related to the three selected domains of Design, Manufacturing and R&D Management. This could be done using a well-considered methodology worked out by an Education and Training Coordination Board consisting of representatives from academia, research centres and industry. Simultaneously, key players on the supply side should be identified and selected by this Board based on specified criteria.

The second step would be to organize a conference at which these requirements and demands are discussed in detail and judged against what is currently on offer from the educational community. The goal would not only be to find obvious matches but also to identify gaps. The procedure and approach of this conference should be worked out by the Board.

Based on the outcome of the conference, the third step would be to work out a roadmap and priority plan for Education and Training with an emphasis on bridging the gaps by well-considered actions.

Managing the actions

In order to set up these initial actions and in order to further manage Education and Training initiatives, it is proposed to install an Education and Training Coordination Board comprising representatives from industry, the academic world and research centres committed to education and training. The first task of this Board should be the preparation and coordination of the actions described in the previous paragraphs including the organization of the conference and the preparation and distillation of an Education and Training plan and roadmap, including all related actions.

This board should have the necessary administrative support within the ENIAC office. In a second phase, the Board should have the authority to supervise and further steer the defined actions. Exploring the most effective ways and scenarios for financing these actions, by relying on existing channels or finding new ones, would also be an important task for the Board. The composition of the board should be such that it ensures a demand-driven approach but with sufficient view on the complementary background and strengths of the different education providers. A board of 9 members with 3 representatives from industry, 3 from academia and 3 from research centres could be envisaged.

Making it happen

With the worldwide nanoelectronics market growing at 8-10% per year, R&D efforts will need to double in the coming decade in order to be able to counter the major challenges lying ahead. Apart from the strategic shifts in technical content indicated above, an increasing fraction of the total effort will have to be dedicated to shared technology R&D and precompetitive advanced research, including investments in research infrastructures and pilot lines. Stimulating such cooperative programmes in Europe will make it possible to limit the overall expense associated with product development and production ramp-up, thereby enhancing world-wide competitiveness for the European industry at large.

Includes operational costs of research infrastructures and pilots

	2005		2015	
	Private	Public	Private	Public
Advanced research	80	175	140	420
Technology integration	490	325	780	780
Application development	1980	0	3390	0
Prototyping	850	0	1290	0
Million Euro per year	**3400**	**500**	**5600**	**1200**

Public-private ratio needs to increase considerably, e.g., to advanced research 75/25, technology integration 50/50

Proposed ENIAC R&D effort sharing through public-private partnerships

Shared R&D efforts through public-private partnerships have proved to be very successful in establishing Europe's position in microelectronics. Extending these partnerships to jointly attack the new challenges of nanoelectronics is the logical way forward. Sharing financing of technology integration on the basis of 50/50 public/private contribution, and advanced research on the basis of 75/25 public/private contribution, is considered a fair overall guide for future programmes. Application development and prototyping are anticipated to be largely covered by private means, as is the case today, which brings the eventual overall percentage of public participation to nanoelectronics R&D to approximately 18%.

Suitable machinery for creating new European infrastructures and ecosystems for nanoelectronics research already exists in the form of the European Commission's Framework Programme and pan-European EUREKA programmes such as MEDEA+, PIDEA, and EURIMUS. Having defined a Strategic Research Agenda for nanoelectronics, the R&D that it identifies as critical to success can be stimulated through these programmes in association with individual member countries. The EC Treaty already includes articles that would allow this coordinated funding to take place between the EU and national R&D programmes.

Implementing the ENIAC Strategic Research Agenda will require a holistic approach in a distributed industrial context of ecosystems. In addition to technological development, ENIAC brings forward proposals for improving the co-ordination of the European research instruments and for fostering efficient innovation environments. By doing so, ENIAC stakeholders ensure that the right research is conducted in the right way.

Structuring research

To achieve its objectives, ENIAC research projects must be both on a large scale and coherent. Maximum use must be made of a wide range of existing RTD European instruments. To enable coherent, co-operative action, ENIAC puts forward a synergetic approach consisting of three pillars under a common roof, as depicted in the figure.

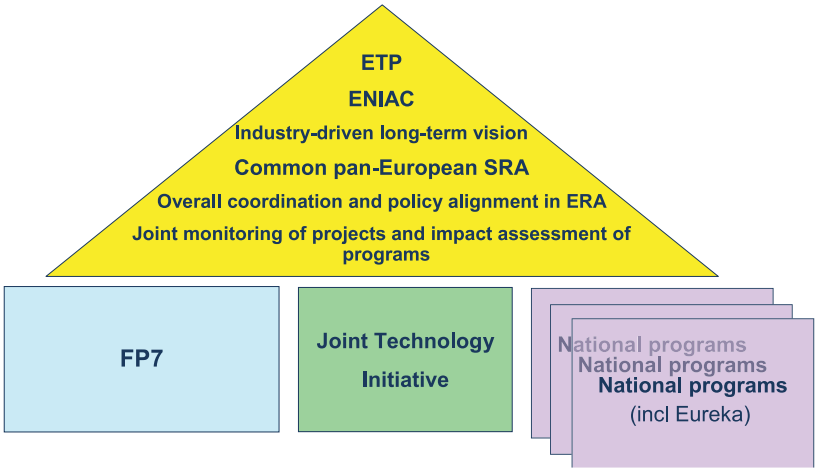
For the first pillar, focussing mainly on the upstream part of the ENIAC SRA, use will be made primarily of the regular instruments in the four Specific Programmes envisaged for FP7, in particular:

- Cooperation: collaborative research projects, Networks of Excellence, coordination of national programmes and international cooperation under the thematic priority ICT
- Ideas: fundamental research on Nanoelectronics funded via the European Research Council
- People: Marie Curie Fellowships for training and public-private mobility of researchers
- Capacities: research infrastructures for promoting the development of world-class Centres of Excellence for Nanoelectronics in Europe; research at universities and institutes for (groupings of) SMEs

To benefit from EU financial support through these instruments, ENIAC stakeholders will participate in the normal Calls for Proposals of FP7. In addition, Centres of Excellence may envisage applying for EU Structural Funds, as well as loans from the European Investment Bank in combination with the new Risk Sharing Facility foreseen in FP7. Furthermore, the new EU Competitiveness and Innovation Programme (CIP) may provide opportunities for SMEs.

For the second pillar, focusing mainly on the downstream part of its SRA, ENIAC proposes setting up a Joint Technology Initiative (JTI). The only means to mobilise the critical mass required for implementing the selected parts of the SRA is a Public-Private Partnership combining private sector resources with national and European public funding. The core of the JTI will be an ITEA/MEDEA+ style industry-driven program for collaborative RTD. In addition, the JTI will provide a flexible basis for common public-private actions to create a fertile ecosystem in Europe for innovation in nanoelectronics, involving large firms, SMEs, institutes and universities.

Regarding the collaborative RTD program, industry will commit to investing the RTD efforts necessary for accomplishing the selected ENIAC SRA objectives. The private sector will contribute in-kind, mainly in the form of RTD staff executing the projects. With 50% of integral RTD costs publicly funded at national and European levels, industry will carry the remaining 50% of the integral RTD costs, as well as the costs and risks of all RTD and innovation in the nanoelectronics domain, beyond the phase of pre-competitive RTD that is publicly supported in the context of ENIAC. Furthermore, industry will cover the organisational costs of governing the JTI and its Operations structure. On the public side, the EU will provide a financial



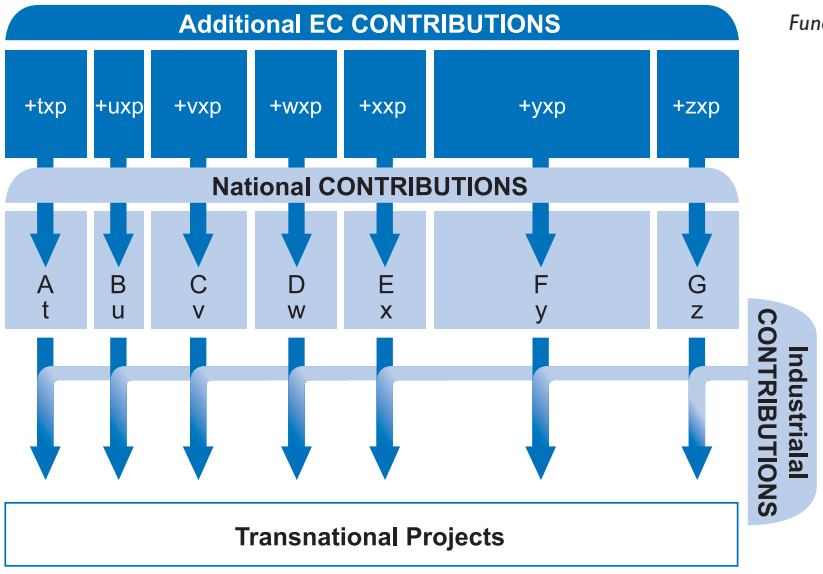
Proposed ENIAC governance model

incentive for Member States to focus national RTD activities in nanoelectronics on the ENIAC SRA; to join forces within the European Research Area; and to improve the efficiency of funding mechanisms for intergovernmental cooperation, in particular the ICT clusters in EUREKA. In essence, an EU contribution will complement the financial contributions from each Member State or Associated State engaged in the JTI to its national participants in transnational projects, as illustrated in the figure below.

Fostering transnational cooperation

The EU contribution will be pre-determined at a fixed percentage of the national contributions. In this way, Member States and Associated States will be stimulated to participate in the JTI, increase their RTD expenditures on nanoelectronics, and cooperate transnationally. In addition, the scheme would optimally exploit the advantages and valuable experiences of EUREKA ICT clusters such as MEDEA+ and ITEA in running industry-driven RTD programmes, while overcoming EUREKA's notorious problem of harmonising and synchronising funding.

For the third pillar, it is anticipated that additional national or even regional activities could take advantage of a certain level of coupling with the ENIAC SRA. This will allow full consistency of the European development work, while ensuring dedicated support where the local impact can be maximised. Alternately, for those countries interested in a more formal inter-governmental scheme, developing bi- or tri-lateral activities will reinforce the coherence of the overall programme, if those activities are well aligned with the ENIAC SRA objectives.



Funding strategy for transnational cooperation

Summary

Building on existing strengths, the European nanoelectronics industry has the potential to be world-class. The knowledge base, high-skill employment and economic success that it will bring will allow Europe to master its own destiny in the way that it uses information society technologies to fulfil societally relevant needs. As an important part of this endeavour, the ENIAC Strategic Research Agenda will identify key research domains and blocking points and provide guidance for creating the public-private partnerships needed to address and overcome them. It will bring large industrial players, academia and SMEs together into clearly focused ecosystems so that they can jointly face the new challenges, and it will help to create coherent structures for national and pan-European sponsorship to achieve timely results.

Although Europe is in a strong position to make the transition from microelectronics to nanoelectronics, the research challenges and infrastructure investment required should not be underestimated. Europe is not the only part of the world to have recognized the importance of the shift. Nanoelectronics research and development networks are already being established in the USA and the Far East, each serving the objectives of their own communities and industries.

This makes it doubly important for all the key players in Europe to work together to ensure the levels of efficiency needed to maintain Europe at the forefront of the nanotechnology revolution. Comprehensively leveraging the knowledge base in Europe is an endeavour that must engage academia and industry alike, bringing together the leading-edge research of universities and research establishments, the specialist knowledge of SMEs and the industrial muscle of large companies to achieve the critical mass needed to achieve breakthrough results. It must be carried out in an environment that promotes the sharing of knowledge and resources, together with the necessary education and training, to achieve common objectives. The cumulative effect will be the creation of a research and manufacturing infrastructure that encourages European nanoelectronics companies to maintain their leading-edge production capabilities firmly in Europe, along with the high-skill jobs that go with them.

More ENIAC information at http://www.cordis.lu/ist/eniac

Glossary

ARTEMIS	ETP on embedded systems
CMOS	Common semiconductor technology for logic switches and integrated circuits
CMP	Chemical-mechanical polishing
DfM	Design for Manufacturing
DMOS	Dedicated high-voltage high-power CMOS
DRAM	Common silicon memory (dynamic random access)
EDA	Electronic design automation
EMC	Electromagnetic compatibility
ENIAC	ETP on nanoelectronics
ERA	European research area
ETP	European technology platform
EUREKA	Pan-European network for market-oriented industrial R&D
EURIMUS	EUREKA cluster on microsystems and MEMS
EUV	Extreme ultraviolet radiation (soft X-ray)
FET	Field-effect transistor (basic device in CMOS)
IC	Integrated circuit (usually made in CMOS)
ICT	Information and communication technology
ITEA	EUREKA cluster on software technology
ITRS	International technology roadmap for semiconductors
JTI	European joint technology initiative
LAN	Local area network
MEDEA+	EUREKA cluster on microelectronics
MEMS	Micro-electromechanical switch
ML2	Mask-less lithography
MuCFET	Multi-channel FET
MuGFET	Multi-gate FET
PIDEA	EUREKA cluster on interconnection and packaging
RF	Radio frequency (operating typically above >1 GHz)
SiP	System in package
SME	Small and medium sized enterprises
SoC	System on chip
SOI	Silicon on insulator technology
SRA	Strategic research agenda
TCAD	Technology-oriented computer aided design